GaN Reliability and Lifetime Projections: Phase 14

Alejandro Pozo Ph.D., Shengke Zhang Ph.D., Gordon Stecklein Ph.D., Ricardo Garcia, John Glaser Ph.D., Zhikai Tang Ph.D., and Robert Strittmatter Ph.D., Efficient Power Conversion

The rapid adoption of GaN devices in many diverse applications calls for continued accumulation of reliability statistics and research into the fundamental physics of failure in GaN devices. This eBook presents the strategy used to measure and predict lifetime based upon tests that force devices to fail under a variety of conditions. This information can be used to create stronger and higher performance products for the industry.

Available for purchase, on EPC's website, is a comprehensive analysis of GaN-based technology, solutions, and applications described in the latest text book: GaN Power Devices and Applications.

NEED FOR ADDITIONAL STANDARD QUALIFICATION TESTING

Why test-to-fail in addition to standard qualification testing?

Standard qualification testing for semiconductors typically involves stressing devices at or near the limits specified in their datasheets for a prolonged period of time, or for a certain number of cycles. The goal of qualification testing is to have zero failures out of a relatively large group of parts tested.

This type of testing is inadequate since it only reports parts that passed a very specific test condition. By testing parts to the point of failure, an understanding of the amount of margin between the datasheet limits can be developed, and more importantly, an understanding of the intrinsic failure mechanisms can be found. By knowing the intrinsic failure mechanisms, the root cause of failure, and the behavior of this mechanism over time, temperature, electrical or mechanical stress, the safe operating life of a product can be determined over a more general set of operating conditions (For an excellent description of this methodology for testing semiconductor devices, see reference [1]).

Key Stress Conditions and Intrinsic Failure Mechanisms for GaN Power Devices

What are the key stress conditions encountered by GaN power devices and what are the intrinsic failure mechanisms for each stress condition?

As with all power transistors, the key stress conditions involve voltage, current, temperature, and humidity, as well as various mechanical stresses. There are, however, many ways of applying these stress conditions. For example, voltage stress on a GaN FET can be applied from the gate terminal to the source terminal (V_{GS}), as well as from the drain terminal to the source terminal (V_{DS}). For example, these stresses can be applied continuously as a DC bias, they can be cycled on-and-off, or they can be applied as high-speed pulses. Current stress can be applied as a continuous DC current, or as a pulsed current. Thermal stresses can be applied continuously by operating devices at a predetermined temperature extreme for a period of time, or temperature can be cycled in a variety of ways.

By stressing devices with each of these conditions to the point of generating a significant number of failures, an understanding of the primary intrinsic failure mechanisms for the devices under test can be determined. To generate failures in a reasonable amount of time, the stress conditions typically need to significantly exceed the datasheet limits of the product. Care needs to be taken to make certain the excess stress condition does not induce a failure mechanism that would never be encountered during normal operation. To make certain this is not the case, the failed parts need to be carefully analyzed to determine the root cause of their failure.

Only by verifying the root cause can a true understanding of the behavior of a device under a wide range of stress conditions be developed. It should be noted that, as more understanding of intrinsic failure modes in eGaN devices is gained, two facts have become clear; (1) eGaN devices are more robust that Si-based MOSFETs, and (2) MOSFET intrinsic failure models are not valid when predicting eGaN device lifetime under extreme or long-term electrical stress conditions.

Stressor	Device/ Package	Test Method	Intrinsic Failure Mechanism
Voltage	Device	HTGB	Dielectric failure (TDDB)
			Threshold shift
		HTRB	Threshold shift
			$R_{DS(on)}$ shift
		ESD	Dielectric rupture
Current	Device	DC Current (EM)	Electromigration
			Thermomigration
Current + Voltage (Power)	Device	SOA	Thermal Runaway
		Short Circuit	Thermal Runaway
Voltage Rising/Falling	Device	Hard-switching Reliability	$R_{DS(on)}$ shift
Current Rising/Falling	Device	Pulsed Current (Lidar reliability)	None found
Temperature	Package	HTS	None found
Humidity	Package	MSL1	None found
		H3TRB	None found
		AC	None found
		Solderability	Solder corrosion
		uHAST	Denrite Formation/Corrosion
Mechanical / Thermo-mechanical	Package	TC	Solder Fatigue
		IOL	Solder Fatigue
		Bending Force Test	Delamination
		Bending Force Test	Solder Strength
		Bending Force Test	Piezoelectric Effects
		Die shear	Solder Strength
		Package force	Film Cracking

Table 1: Stress Conditions and Intrinsic Failure Mechanisms for eGaN FETs

FOCUS AND STRUCTURE OF THIS REPORT

Table 1 lists in the left-hand column all the various stressors to which a transistor can be subjected during assembly or operation. Using the various test methods listed in the third column from the left, and taking devices to the point of failure, the intrinsic failure mechanisms can be discovered. The failure mechanisms confirmed as of this writing are shown in the column on the right.

The first topic discussed in this report, *Section 1: Voltage/Temperature Stress on the Gate (page 3)*, is the intrinsic failure mechanisms impacting the gate electrode of GaN devices. In this section a physics-based lifetime model with supporting evidence is shown. This is a refinement of the more simplistic time- dependent dielectric breakdown model previously used to project the lifetime of a device.

The second topic, *Section 2: Voltage/Temperature Stress on the Drain (page 8)*, discusses the intrinsic mechanisms underlying dynamic $R_{DS(on)}$. The topic of dynamic $R_{DS(on)}$ has garnered much attention from design engineers, reliability experts, and academics. In this section, the key mechanisms are separated and how the understanding of these mechanisms can be used to create more robust devices is shown. As with the gate stress section, the work on dynamic $R_{DS(on)}$ is enhanced through the development of a physics-based model that explains all known behaviors in eGaN transistors relating to changes in $R_{DS(on)}$. This model is therefore most useful for predicting lifetimes in more complex mission profiles.

Section 3: Applying the Model to Common Real-World Use Cases (page 18) applies these data-driven models into real world cases.

Section 4: Safe Operating Area (page 24) focuses on the safe operating area (SOA) of GaN devices. This subject has been studied extensively in silicon-based power MOSFETs, where a secondary breakdown mechanism is observed that limits their utility under high drain bias conditions [2]. Several GaN products were tested exhaustively throughout their datasheet SOA, and then taken to failure to probe the safety margins. In all cases, the data shows that GaN transistors will not fail when operated within the datasheet SOA.

In *Section 5: Short-Circuit Robustness Testing (page 25)*, eGaN devices are tested to destruction under short-circuit conditions. The purpose is to determine how long and what energy density they withstand before catastrophic failure. This information is vital to industrial power and motor drive engineers needing to include short-circuit protection in their designs.

GaN devices have been extensively applied in light detection and ranging (lidar) equip- ment used on autonomous cars, truck, robots, and drones. The fast-switching speed, small size, and high pulsed current capabilities of GaN devices add to a lidar system's ability to "see" at a greater distance with higher resolution. Lidar systems push the limits of dynamic voltage and current (di/dt and dv/dt) beyond anything experienced in silicon.

In *Section 6: High di/dt Current Pulse Reliability (Lidar Application) (page 27)*, a custom test system to assess eGaN reliability over long-term lidar pulse stress conditions is described. As of the date of this writing, devices have passed over thirteen trillion pulses (about triple a typical automotive lifetime) without failure or significant parametric drift.

In *Section 7: Mechanical Stress (page 29)*, the subject of mechanical force testing of wafer level chip-scale (WLSC) packages is presented. Test-to-fail results for die shear (in-plane force) demonstrate robustness that exceeds MIL-STD-883E recommendations. Backside pressure (out-of-plane) tests show the package is capable of 400 psi without failure.

Bending-force tests examine both solder joint robustness and look for any piezoelectric effects that might modulate device electrical parameters. All devices passed a 4-mm deflection (250 N) based on the Q200-005A test standard, with first failures occurring at 6-mm deflection. No electrical parameter changes could be measured. At the end of the section, it is shown that the bending forces required to physically break the devices are well below forces required to change electrical characteristics due to modulation of the piezoelectrically generated fields.

Section 8: Thermo-Mechanical Stress (page 31) examines the issue of thermo-mechanical stresses generated by both temperature cycling and cycling based on self-heating. An extensive study of underfill products was conducted to experimentally generate lifetime predictions. A finite element analysis at the end of this section explains the experimental results and generates guidelines for selection of underfill based on key material properties.

SECTION 1: VOLTAGE/TEMPERATURE STRESS ON THE GATE

1.1 Prior Work

Figure 1 is an example of a Weibull plot of gate failures in an EPC2212 [3] eGaN® FET from Efficient Power Conversion (EPC). The horizontal axis shows the time to failure. The vertical axis shows the cumulative failure probability for different stress conditions applied to the gate.

The plot on the left has different voltages at room temperature and the plot on the right shows two different voltages applied at 120°C. Note that this device has a datasheet maximum gate voltage rating of 6 V, yet very few devices are failing even after many hours at 8 V.

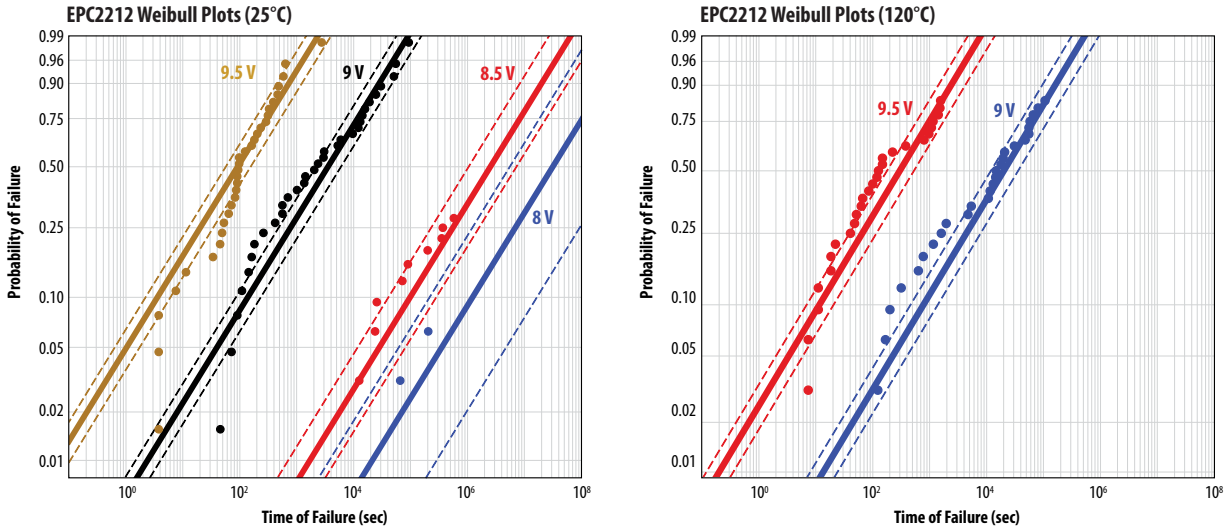


Figure 1: Weibull plots of gate-to-source failures of EPC2212. Note that very few failures occur even at 8 V_{GS}, yet the device has a maximum V_{GS} rating of 6 V. The data on the top is at 25°C and the data on the bottom is at 120°C.

In Figure 2 these data have been translated into failure rates. On the left is the mean time to failure (MTTF) for these same devices versus V_{GS} at both 25°C and 120°C. On the right is a graph that shows the various probabilities of failure versus V_{GS} at 25°C. Note that the failure rate is not very sensitive to temperature but is very sensitive to V_{GS}. Curves were fit to the data points assuming a simple Time Dependent Dielectric Failure Mechanism (TDDB) [3].

Looking at the graph on the right, with a V_{GS} of 6 V_{DC}, which is the absolute maximum allowed voltage for this part one could expect between 10 and 100 parts per million (ppm) failures in 10 years. The recommended gate drive voltage, however, is 5.25 V and the expected failure rate at that voltage is less than 1 ppm in 10 years.

These conclusions are only valid if the primary failure mechanism is the same under all these conditions. To confirm this, failure analysis was performed on multiple parts from this study, and a consistent failure mode was found. Referring to the image in Figure 3, the yellow circle indicates the failure site is between the gate metal and the metal 1 layer. These two layers are separated by a silicon nitride dielectric layer. It is this silicon nitride layer that failed, not any of the GaN layers beneath.

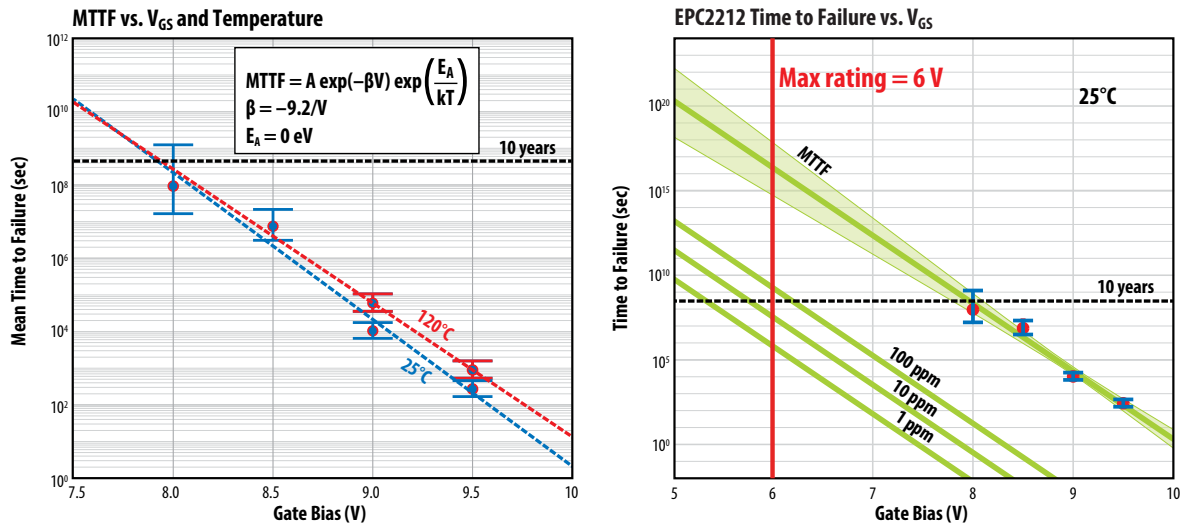


Figure 2: On the left is the mean time to failure (MTTF) for EPC2212 eGaN FETs versus V_{GS} at both 25°C and 120°C. On the right is a graph that shows the various probabilities of failure versus V_{GS} at 25°C.

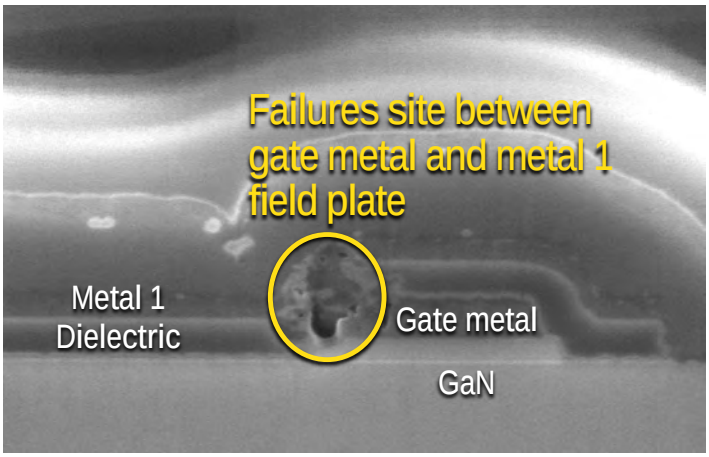


Figure 3: Scanning electron microscopy (SEM) image of the gate region of an EPC2212 eGaN FET. The yellow circle shows the failure site is between the gate metal and the metal 1 layer.

While this lifetime study provided a solid phenomenological model of gate reliability in eGaN FETs, many fundamental questions remained unanswered:

- Why does dielectric rupture occur in a high-quality silicon nitride film at an electric field well below its breakdown strength? And, why does this rupture occur at the corner of the gate?
- Why does gate lifetime increase as temperature rises?
- Is the exponential scaling of MTTF with gate voltage truly applicable to eGaN FETs? Is there perhaps a different mathematical model that is predicated on the root physics of failure in GaN?

To resolve these questions, EPC conducted more extensive gate acceleration studies on recent lots of EPC2212 devices, using larger sample sizes and longer durations (> 1000 hours in some cases). In addition, several core experiments to uncover the dynamics of failure at high gate bias were performed. These studies resulted in an improved understanding of the physics of failure and, for the first time, an *ab initio* lifetime equation specific to eGaN technology that is derived directly from this physics.

EPC has gathered convincing evidence that gate failure at high bias in eGaN FETs is caused by a two-step process. In the first step, impact ionization inside the p-GaN gate layer leads to the production of electron-hole (e-h) pairs. Some of these holes scatter and trap in the Si_3N_4 layer near the corner(s) of the gate. Over time, as this trapped hole charge density accumulates, the electric fields in the dielectric grow until, at a certain critical charge density, it ruptures catastrophically.

The result of this dynamic is the five-parameter gate lifetime equation shown in Equation 1:

$$MTTF(V_{GS}, \Delta T) = \frac{A}{(1 - c\Delta T)} exp\left[\left(\frac{B}{V_{GS} + V_0}\right)^m\right] \quad \text{Eq. 1}$$

where V_{GS} is the gate voltage and ΔT is the temperature (relative to 25°C). The remaining parameters in Equation. 1 are provided in the table below:

$m =$ 1.9
$V_0 =$ 1.0 V
$B =$ 57.0 V
$A =$ 1.7×10^{-6} s
$c =$ 6.5×10^{-3} K^{-1}

1.2 Physics-Based Derivation of Gate Lifetime Model

In this section, a theory outlined above and a corresponding lifetime model to explain the physics of failure of GaN transistors under high gate bias is derived. The result is a practical equation for estimating reliability under various conditions. This equation is derived from, and applicable to the unique device physics of enhancement-mode GaN gates, rather than borrowed from the generic reliability models for Si MOSFETs.

To lay the groundwork for this theory, a host of basic experiments aimed at clarifying the root cause of gate failure were conducted. For the lowest voltage legs, the total stress period exceeded 2000 hours, allowing the generation of more failures and tightened statistical confidence intervals. In addition, the breakdown strength of the of Si_3N_4 dielectric layer was thoroughly characterized, using dedicated test structures and alternating field direction. Finally, electro-luminescence (EL) studies were conducted on devices to understand the dynamics in time leading up to catastrophic gate rupture.

A successful model of gate failure in GaN transistors must account for the following key observations:

Dielectric Failure is Observed in the Si_3N_4 Straddling the Sidewall of the pGaN Gate

The failure can occur on either the source or drain sidewall.

- The same Si_3N_4 film, when measured on test structures isolated from the pGaN gate, does not fail until a field strength much larger (6x) than experienced during 10 V gate stress. This is true no matter the polarity of the field inside the dielectric.
- The gate failure rate shows a negative temperature coefficient. This is surprising because both gate leakage and time-dependent dielectric breakdown (TDDB) typically show a positive temperature coefficient.
- The measured MTTF shows very high acceleration with gate bias. Furthermore, the marginal acceleration is not constant with gate bias, which is inconsistent with a simple exponential acceleration law. The acceleration is steepest at lower V_{GS}, and levels off at high bias.
- High energy (> 2 eV) photon emission is seen at a localized point along the gate in the time interval leading up to gate failure. Subsequent failure analysis reveals dielectric rupture at the exact same location.

As a result of these collective observations, a multi-step process was theorized to be responsible for gate failure at high V_{GS}. This process is depicted schematically in Figure 4. In the first step, electrons are injected into the pGaN gate layer from the 2DEG. They are injected via tunneling or thermionic emission over the AlGaN hetero-barrier [5]. Once inside the pGaN layer, the electrons gain energy rapidly from the electric field, with some gaining sufficient energy to cause impact ionization. This leads to the generation of electron-hole pairs, particularly in the high field region just under the gate metal.

In the second step of this process, holes move away from the gate metal under the influence of the field. Near the sidewall of the gate, a certain fraction of holes scatter into the Si_3N_4 dielectric, where they become trapped in deep states. This process is aided by the fact that the Si_3N_4/GaN interface has a Type II staggered band alignment [6, 7], whereby the valence band maximum in Si_3N_4 is higher than in GaN. This means holes generated in GaN near the interface have no (or low) barrier for emission into the dielectric.

In the final step of this process, holes become trapped in the dielectric, leading to a growing positive charge density Q_h. This charge, in turn, leads to an increasing electric field in the dielectric between the metal field plate and gate metal in the vicinity of the gate sidewall. Once this charge density reaches a critical density (Q_c), the dielectric ruptures, leading to the kind of catastrophic damage near the sidewall observed in failure analyses of gate failures [8].

The failure mode is a charge-to-failure type model of dielectric breakdown. However, the charge is accumulated from impact ionization in the neighboring pGaN layer, not from leakage through the dielectric itself. Therefore, the dynamics of this multi-step process is mediated by the rate-limiting step of impact ionization in GaN. Consequently, the gate lifetime can be modeled by using the equations of impact ionization in GaN, which are developed in the sections to follow.

Figure 5 (top) shows a band-diagram of an GaN gate under high forward bias (9 V). In this diagram, the far left corresponds to the gate metal, while the AlGaN barrier can be seen toward the right. Note that electron-hole pair production from impact ionization is depicted in the highest field region near the gate metal. Figure 5 (bottom) plots the corresponding electric field within the gate for the same conditions. Note that the field is not uniform, reaching a maximum near the gate metal. For 9 V gate bias, the peak field exceeds 2 MV/cm. This field strength is sufficient to allow for stable impact ionization (but not avalanche breakdown) in GaN [9, 11]. This is particularly true in regions where fields might be slightly concentrated, such as near threading dislocations, stress concentrations, or small troughs in surface morphology.

1.3 E-Field Dependence on Gate Voltage

Figure 6 shows the simulated E-field inside the pGaN gate as a function of forward gate bias. Both the maximum (near the gate metal) and average E-fields are shown. The fields were calculated using a non-equilibrium 1-D Fermi-Poisson solver [12]. At low bias, the field is dominated by built-in piezoelectric charges. At higher bias, the E-field grows linearly with V_{GS}, where the proportionality constant is the gate thickness, d. Note that d includes both the pGaN thickness as well as the AlGaN thickness. The equation inset in Figure 6 gives a simple model for field F vs. V_{GS} that will be used later.

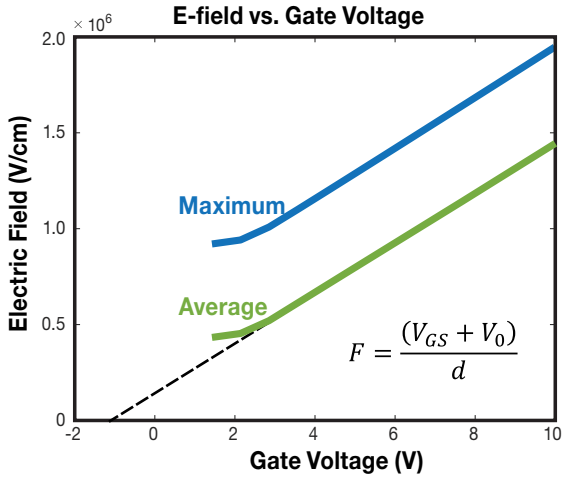


Figure 6: E-fields inside the pGaN gate as a function of forward gate bias. Both the maximum (near the gate metal) and average E-fields are shown. Dashed line shows simple offset linear model for field F vs. V_{GS}. The parameter V_0 is the built-in voltage, and d is the effective gate thickness.

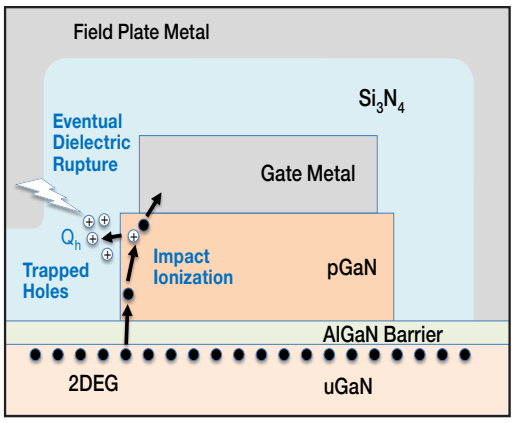


Figure 4: Schematic of gate failure mechanism in an GaN transistor. A small current of electrons tunneling through the AlGaN front barrier enter the pGaN gate region, where they are accelerated in high fields toward the gate metal. A small percentage gain sufficient energy to cause impact ionization, particularly near the gate metal. The resulting holes are mostly swept away, but some trap and accumulate in the Si_3N_4 dielectric layer. Once sufficient trapped hole density, Q_h, has accumulated, fields concentrate in the dielectric, ultimately leading to catastrophic rupture

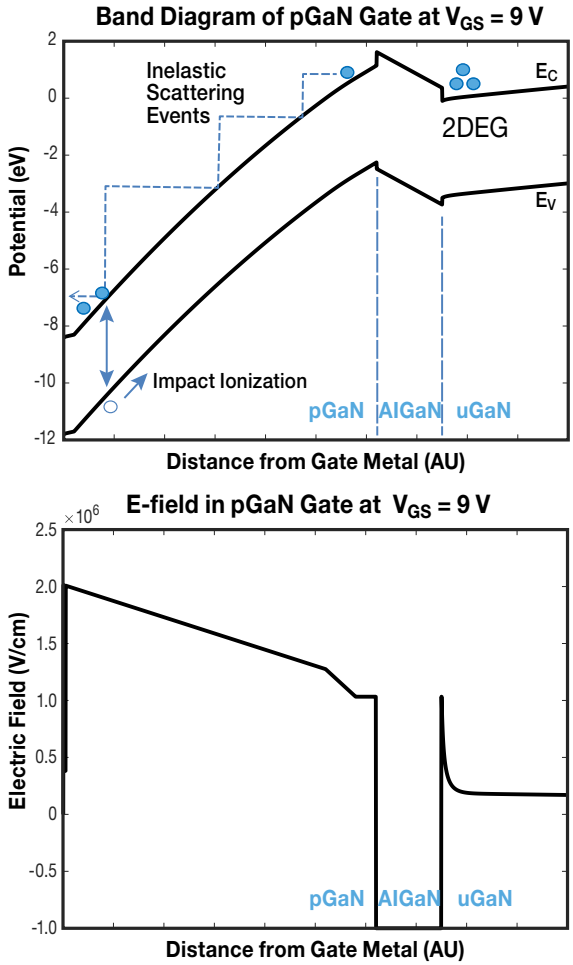


Figure 5: Band-diagram of pGaN gate under high forward bias (9 V) (left). Far left corresponds to the gate metal; AlGaN front barrier is seen toward the right. Note that electron-hole pair production is depicted in the high field region near the gate metal. Electric field in the gate for the same conditions (right). Note the field is not uniform, reaching a peak > 2 MV/cm.

In the development to follow, the average field, as opposed to the maximum field is used. Even though impact ionization is strongly accelerated with electric field, the physics of impact ionization requires a certain mean free path (or dead space) for electrons to gain sufficient kinetic energy to cause electron-hole pair generation. This mean free path is on the order of the gate thickness. Therefore, the field throughout the gate (or average field) is a more appropriate input variable to calculate impact ionization.

Models of Impaction Ionization in GaN

The electron-hole pair generation rate from impact ionization is modeled by the following equation [13]:

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q} \quad \text{Eq. 2}$$

where G is the electron-hole generation rate (#/cm^3), J_n and J_p are the electron and hole currents (A/cm^2), and α_n and α_p are the electron and hole impact ionization coefficients (#/cm). The ionization coefficient gives the number of electron-hole pairs created in a unit distance (1 cm) traveled by the electron/hole. These coefficients are strongly E-field and temperature dependent.

The field dependence of the ionization coefficients in GaN have been studied by several authors using either first principles full-band Monte Carlo simulations or via experimental measurement on avalanche photodiodes [13]. All of these studies employed Chynoweth's form [15] for the electron ionization coefficient widely used in other semiconductors:

$$\alpha_n = \alpha_n e^{-(b_n/F)^m} \quad \text{Eq. 3}$$

where F is the electric field, and α_n, b_n, and m are parameters. This equation, which provides an excellent fit to both simulations and measurements, is strongly accelerated by the electric field, particularly in the intermediate range of field strength seen inside a pGaN gate. Table 2 compares Chynoweth's parameter values for GaN from several references.

Ref	a_n (1/cm)	b_n (V/cm)	m
Ji et al.[10]	2.10E+09	3.70E+07	1
Ozbek [14]	9.20E+05	1.70E+07	1
Cao et al. [9]	4.48E+08	3.40E+07	1
Ooi et al. [16]	7.32E+07	7.16E+06	1.9

Table 2: Comparison of Chynoweth's parameters for impact ionization in GaN. Note: Information from several authors, employing either ab-initio simulations or direct measurements.

All parameter values yielded similar results when fit to our gate lifetime data. In the end, the form provided by Ooi [16] is chosen for two reasons: (1) close agreement with several independent publications [13, 17], and (2), as will be shown shortly, the parameters quoted provided a near exact match with our experimental data.

1.4 Temperature Dependence

The temperature dependence of avalanche breakdown in GaN has been disputed by various groups, with some reporting positive while others reporting negative temperature coefficients [18]. More recently, a consensus in both theoretical (full-band Monte Carlo simulations) and experimental data has emerged that the impact ionization rates for both electrons and holes drop as temperature rises. This means that ionization (and avalanche breakdown) is more likely to occur at low temperature. The main reason for this is the role of phonon scattering on the mean free path of carriers. At high temperature, increased scattering reduces the mean free path and therefore the kinetic energy carriers can absorb from the electric field. With fewer high energy carriers, the rate of ionizing collisions (i.e., impact ionization) is reduced accordingly. Note that the increased MTTF at high temperature observed in the gate reliability data is somewhat unusual in the physics of failure and is strongly suggestive that impact ionization is playing a fundamental role.

Ozbek [14] studied the temperature dependence of the impact ionization coefficients in GaN in the temperature range 300 K to 400 K using the electron beam induced current (EBIC) methodology. He found a clear monotonic (and negative) response. Ozbek found that the Chynoweth's coefficients b_n and m in Equation 4 did not change with temperature, whereas the coefficient a_n did change. He fit the measured response to a simple linear temperature dependence as shown in Equation 4.

$$a_n(T) = a_{n;0}(1 - c\Delta T) \quad \text{Eq. 4}$$

where c = 6.5 x 103 K-1 and ΔT (in Kelvin) is the temperature rise above 300 K. This temperature dependence is employed in the model to follow.

Final Lifetime Equation

At this stage, we have all the of the mathematical ingredients to derive a lifetime equation applicable to pGaN gates. As a first step, we note that the generation rate equation (Equation 2) can be simplified to:

$$G \approx \alpha_n \frac{|J_n|}{q} \quad J_n \gg J_p \quad \text{Eq. 5}$$

where we have neglected the contribution from hole-initiated ionization. This is valid because unlike electrons which tunnel through the AlGaN barrier under forward bias, no holes are injected into the gate region. There is no sustained source or injecting contact for holes in a GaN gate. Furthermore, though holes are generated at a low rate via electron-initiated impact ionization, the corresponding current (and multiplication) of holes is orders of magnitude lower than the electron current.

Most of the generated holes are swept away toward the AlGaN barrier, but some trap in the Si_3N_4 dielectric layer in the vicinity of the gate sidewall. As the positive (hole) charge accumulates in the dielectric over time, the fields near the field plate edge grow as well (see Figure 4). Once a certain critical charge density has accumulated (denoted Q_c), the fields in the dielectric will reach breakdown strength, and the Si_3N_4 will rupture from field plate to pGaN gate (or gate metal).

If it is assumed that the hole generation rate (from electron-initiated impact ionization) does not vary with time as charge accumulates in the dielectric, the mean time to dielectric failure will simply be:

$$MTTF \propto \frac{Q_c}{G} \quad \text{Eq. 6}$$

By combining Equation 6 with Equations 3, 4, and 5, an expression for the MTTF as a function of temperature and field in the gate is obtained:

$$MTTF = \frac{Q_c}{G} = \frac{qQ_c}{\alpha_n J_n} = \frac{qQ_c}{J_n a_{n,0}(1 - c\Delta T)} exp\left[\left(\frac{b_n}{F}\right)^m\right] \quad \text{Eq. 7}$$

Note that the implicit assumption was made that the injection rate J_n, and the vertical electric fields F do not change appreciably as trapped hole charge builds up in time.

$$MTTF = \frac{Q_c}{G} = \frac{qQ_c}{\alpha_n J_n} = \frac{A}{(1 - c\Delta T)} exp\left[\left(\frac{B}{V + V_0}\right)^m\right] \quad \text{Eq. 8}$$

Inserting the field dependence on gate voltage (from Figure 6), and lumping together parameters where possible, results in the final 5-parameter gate lifetime model:

with parameters listed: $m = 1.9$
$V_0 = 1.0\ V$
$B = 57.0\ V$
$A = 1.7 \times 10^{-6}\ s$
$c = 6.5 \times 10^{-3}\ K^{-1}$

In the last step resulting in Equation 8, the gate voltage and temperature impact on the injection current J_n were neglected, treating it as a constant. While gate leakage does increase monotonically with both V_{GS} and ΔT, the measured dependence is weak in comparison with the large voltage acceleration caused by impact ionization (as captured by Chynoweth's equation). While the voltage dependence of J_n could be added to the model at the expense of making it more complicated, the result would be to add only slightly to the already large acceleration in MTTF vs. V_{GS}.

The lifetime equation (Equation 8) is plotted against measured acceleration data for EPC2212 in Figure 7. Note that the non-uniform acceleration with voltage of the model matches the data well. This voltage acceleration appears as curved rather than linear when viewed in log-linear space. To produce this fit, we fixed all parameters in Equation 8 except *A* and *B*. The resulting best fit for *B*, (when converted into a field by dividing by the gate thickness *d*), resulted in a value of $b_n = 7.6 \times 10^6$ V/cm, in very close agreement with Ooi's value of 7.2×10^6 V/cm [14]. Figure 8 shows the temperature dependence of the lifetime equation at –75°C, 25°C, and 125°C. The temperature dependence (contained in the parameter *c*) is taken directly from Ozbek without fitting to data. Note that at higher temperature, the MTTF is slightly higher, as observed in the measurements shown in Figure 7.

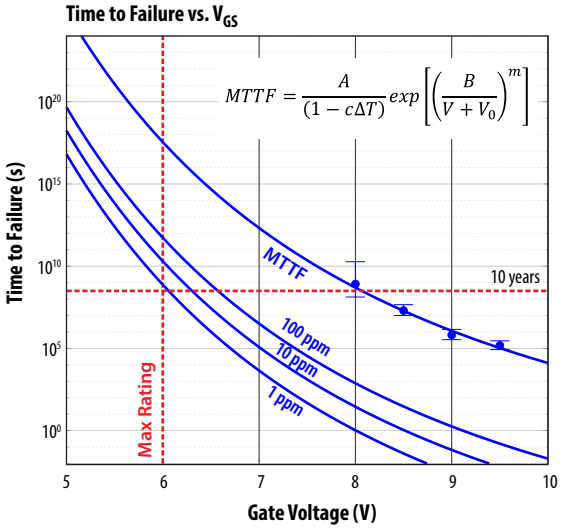


Figure 7: EPC2212 MTTF vs. V_{GS} at 25°C MTTF (and error bars) are shown for four different voltage legs. The solid line corresponds to the impact ionization lifetime model. Extrapolations of time to failure for 100 ppm, 10 ppm, and 1 ppm are shown as well.

1.5 Summary of Physics-Based Derivation of Gate Lifetime Model

The impact ionization model of gate lifetime in GaN transistors (Equation 1) successfully accounts of a host of observed factors:

Positive temperature coefficient of MTTF (which is unusual in semiconductor physics of failure).

- Very high acceleration with gate bias, and acceleration that is steeper than exponential at decreasing gate bias.

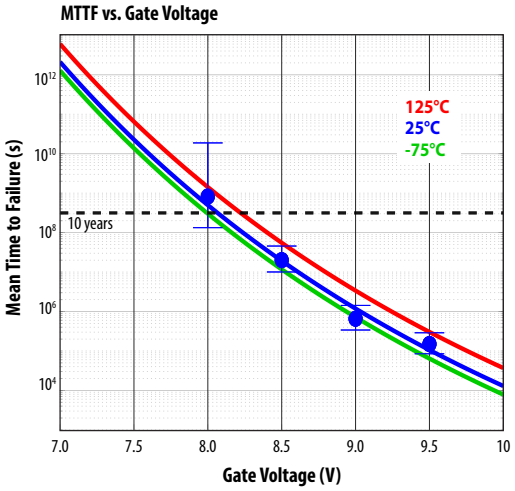


Figure 8: Measured MTTF for EPC2212 (25°C) measured at four different gate biases. Blue line is lifetime model. Red and green lines are predictions of the lifetime model at 125°C and –75°C respectively.

- Dielectric rupture through a high quality Si_3N_4 film at a nominal field strength well below breakdown (as a result of hole injection and trapping from the adjacent pGaN region).

This lifetime equation is not simply borrowed from the body of standard reliability models developed for MOSFETs. Instead, it represents the first gate lifetime model, built up from the root physics of failure, specifically applicable to GaN transistors.

Figure 9 shows a comparison of: (red) the original gate acceleration data and simple exponential acceleration fit based on time-dependent dielectric breakdown only; (blue) recent acceleration data and impact ionization lifetime model. Note that the recent data shows improved measured lifetimes at every voltage, attributable to steady improvements in uniformity and process controls in manufacturing. The impact ionization model (Equation 1) projects longer time to fail at lower V_{GS} within the datasheet range. In particular, the expected time to 1 ppm failure at 6 V (datasheet maximum) exceeds 10 years.

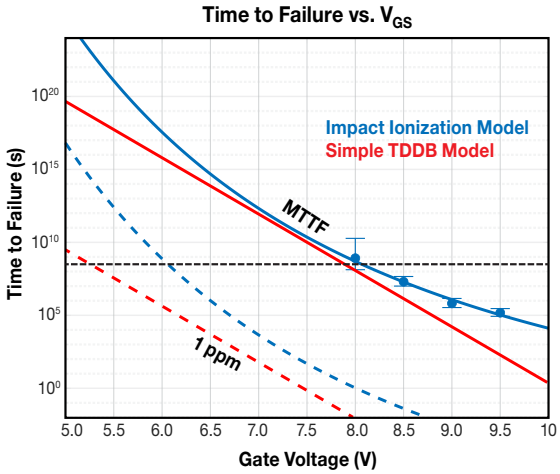


Figure 9: EPC2212 MTTF vs. V_{GS} at 25°C MTTF (and error bars) are shown for four different voltage legs. The solid line corresponds to the impact ionization lifetime model. Extrapolations of time to failure for 100 ppm, 10 ppm, and 1 ppm are shown as well.

SECTION 2: VOLTAGE/TEMPERATURE STRESS ON THE DRAIN

This same methodology can be adapted to every other stress condition. For example, one common concern among GaN transistor users is dynamic on-resistance. This is a condition whereby the on-resistance of a transistor increases when the device is exposed to high drain-source voltage (V_{DS}). The traditional way to test for this condition is to apply maximum-rated DC V_{DS} at maximum-rated temperature (typically 150°C). If there are no failures after a certain amount of time – usually 1000 hours – the product is considered good.

The dominant mechanism causing the on-resistance to increase is the trapping of electrons in trap-states near the channel. As the trapped charge accumulates, it depletes electrons from the two-dimensional electron gas (2DEG) in the ON state, leading to an increase in $R_{DS(on)}$. By applying DC V_{DS} at maximum temperature, the electrons available to be trapped come from the drain-source leakage current, I_{DSS}. In order to accelerate trapping, devices can be taken to voltages above their rated maximum, as shown in Figure 10 for a fourth-generation, 100 V-rated EPC2212 GaN transistor. The data were fit by three-parameter Weibull distribution [19].

In Figure 11, these data have been translated into time-to-fail graphs versus voltage and temperature. On the right side of the graph is shown the time for 1 ppm failures at the maximum rated V_{DS} over 10 years. What is unusual, however, is that the graph on the left shows that the failure rates are not very sensitive to temperature and that the failure rates, although extraordinarily low under all conditions, are lower at 90°C than at either 35°C or 150°C. It will be shown later in this report that this can be explained by understanding that the primary failure mechanism is hot-electron trapping.

Figure 12 is a magnified image of an EPC2016C GaN transistor showing thermal emissions in the 1–2 µm optical range. Emissions in this part of the spectrum are consistent with hot electrons and their location in the device is consistent with the location of the highest electric fields when the device is under drain-source bias.

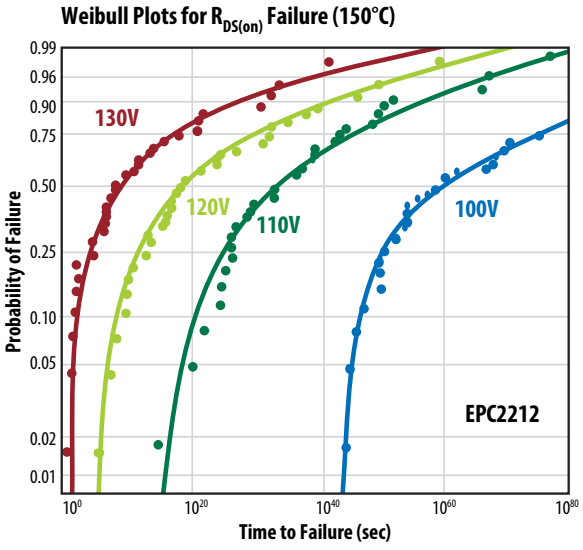


Figure 10: Weibull plot of EPC2212 eGaN FETs stressed under DC bias at various voltages. A failure is defined as exceeding data sheet limits.

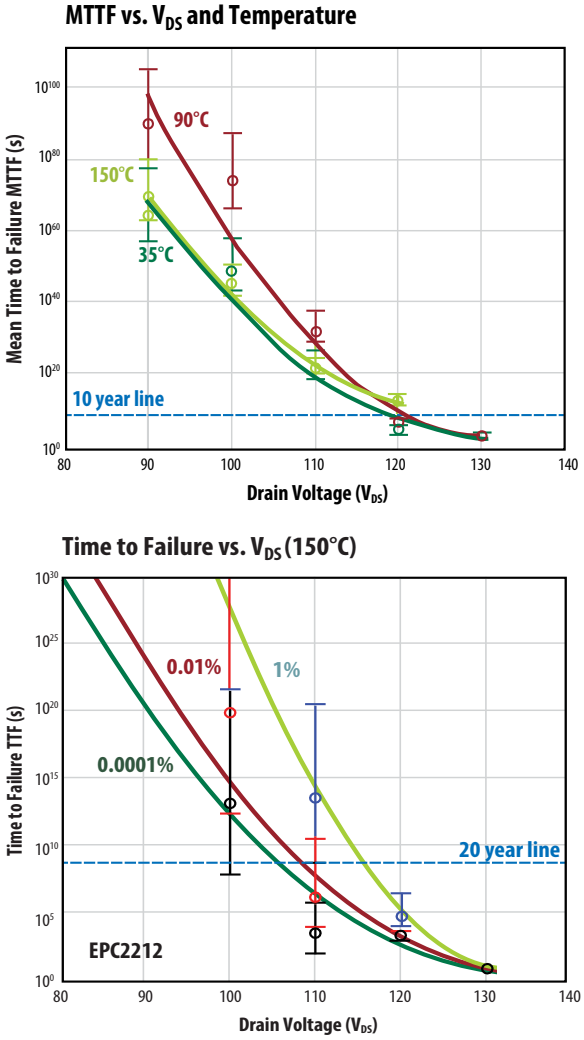


Figure 11: The data in Figure 10, as well as similar data taken at different temperatures, is translated into predictions of failure rates over time, temperature, and voltage.

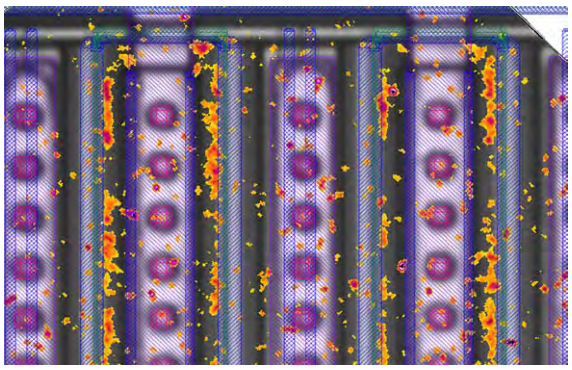


Figure 12: A magnified image of an EPC2212 eGaN FET showing light emission in the 1–2 µm wavelength range (SWIR) that is consistent with hot electrons. The SWIR emission (red-orange) has been overlaid on a regular (visible wavelength) microscope image.

Knowing that hot electrons in this region of the device are the source of trapped electrons, a better understanding of how to minimize the dynamic on-resistance can be achieved with improved designs and processes. By understanding the general behavior of hot electrons, their behavior over a wider range of stress conditions can be generalized.

In addition, by providing more hot electrons, the trapping mechanism can be accelerated. To accomplish this, the circuit shown in Figure 13 that pushes high I_{DSS} through the device at maximum rated V_{DS} was created. In other words, instead of just using the leakage current generated by DC bias at high temperatures as the source of electrons that can get trapped, orders of magnitude more trapping candidates can be generated independent of temperature by making a switching circuit such as shown in Figure 13. This circuit is one of the proposed hard-switching topologies by JEDEC JEP173 [20].

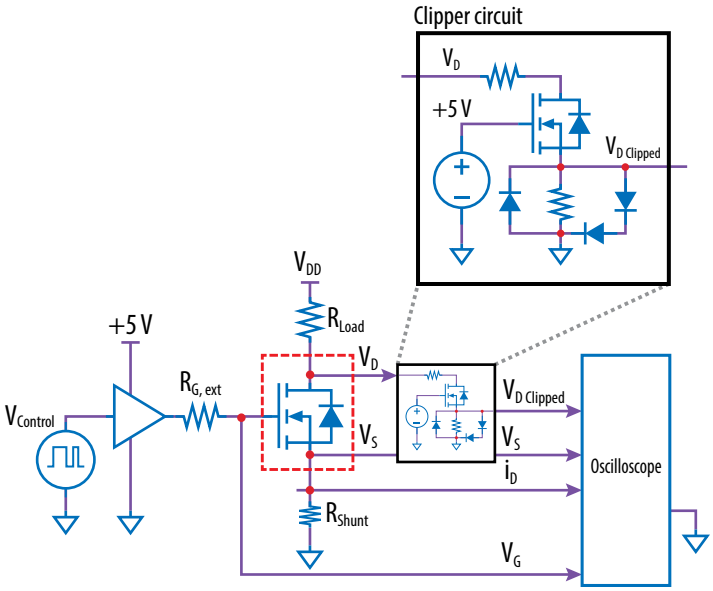


Figure 13: Hard-switching circuit consistent with JEDEC JEP173 [16]

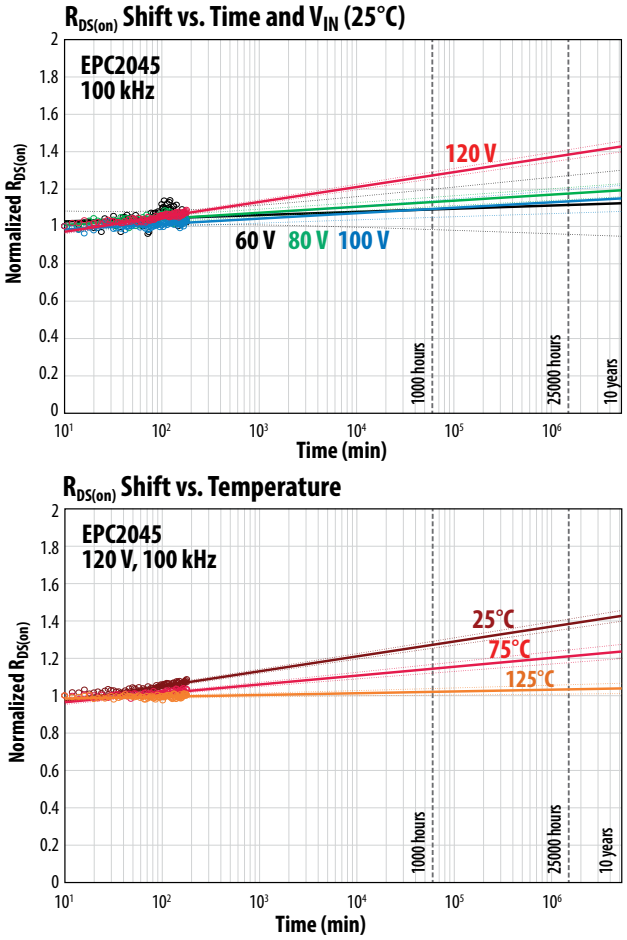


Figure 14: The $R_{DS(on)}$ of a fifth-generation EPC2045 eGaN FET over time at various voltage stress levels and temperatures. On the left, the devices were tested at 25°C at voltages from 60 V to 120 V. The graph on the right shows the evolution of $R_{DS(on)}$ at 120 V at various temperatures.

Figure 14 shows how the $R_{DS(on)}$ of a fifth-generation EPC2045 eGaN transistor [1921], designed with the knowledge that hot electrons trapping is accelerated with peak electric fields near the drain, increases over time at various voltage stress levels and temperatures. The top graph, shows the devices tested at 25°C at voltages from 60 V to 120 V (EPC2045 has a $V_{DS(max)}$ of 100 V). The horizontal axis shows time measured in minutes, with the right side ending at 10 years.

The bottom graph shows the evolution of $R_{DS(on)}$ when biased at 120 V at different temperatures. The counter-intuitive result shows that the on-resistance increases faster at lower temperatures. This is consistent with hot-carrier injection because hot electrons travel further between scattering events at lower temperatures and therefore are accelerated to greater kinetic energies by a given electric field. The result is that the electrons can get to different layers where they are more prone to become trapped. This suggests that traditional testing methods, whereby a device is tested at maximum voltage and temperature, may not be enough to determine the reliability of a device.

The results in Figure 11 can now be better understood. As the device is heated under DC bias, the leakage current increases. The shorter mean free path of the hot carriers, however, counters the increase in available electrons such that the $R_{DS(on)}$ increase over time climbs from room temperature to 90°C, but then starts declining at higher temperatures – another counter-intuitive result.

The publication of these results in Phase 10 and Phase 11 reports has led to great interest in the eGaN community, along with many questions and some skepticism as well.

Key questions to address are:

- Has the log(time) growth characteristic been verified over longer intervals of time? This is important because this growth characteristic is central to long-term lifetime projections.
- How does $R_{DS(on)}$ respond at the low end of the datasheet temperature range (e.g. –40°C)
- How does dynamic $R_{DS(on)}$ compare between inductive and resistive hard switching?
- How does $R_{DS(on)}$ depend on switch current and switching frequency?
- Is there a device physics-based theory to explain the log(time) growth characteristic, as well as the observed temperature and voltage response?
- Can this theory lead to a compact mathematical model that predicts dynamic $R_{DS(on)}$ under different drain voltages and temperatures?

The remainder of this section addresses each of these questions in turn. Long-term dynamic $R_{DS(on)}$ data over more than 1000 hours of continuous hard-switching operation will be shown. Data comparing inductive versus resistive hard-switching will be provided. The effect of low temperature operation (–30°C) and the effect of different switch currents will be demonstrated. At the end of this section, a first principles physics-based model of dynamic $R_{DS(on)}$ in GaN transistors will be provided. This model successfully accounts for all the phenomena mentioned above.

2.1 Continuous Hard Switching Beyond 1000 Hours

The resistive hard-switching system was used to test six samples of EPC2218 GaN transistors simultaneously for over 1000 hours of continuous operation. The purpose of this test is to show that the charge trapping mechanism responsible for a long-term increase of $R_{DS(on)}$ follows a log(time) trend. If this trend is maintained over the long-term, then data from the first few hours can be used to project the expected $R_{DS(on)}$ after 10 or 15 years. Figure 15 shows the normalized $R_{DS(on)}$ over time of all the samples under test, and Figure 16 shows the difference between the line fits using either the first five hours of data, or the full 1150 hours.

The main source of error in the five-hour line fits are small temperature changes in the ambient temperature. These (random) temperature fluctuations tend to cancel out as the length of the test increases. Nevertheless, the short duration and long duration tests agree to within 10% on the projected $R_{DS(on)}$ after 15 years. This lends credence to the idea that short-term data collection (over a few hours) can be used to accurately project long-term dynamic $R_{DS(on)}$ behavior. As will be shown in the later physics-based model, this log (time) extrapolation is valid when the changes in $R_{DS(on)}$ are relatively small. When the changes are larger, the case where a sizeable percentage of the available 2DEG electrons are trapped, there needs to be a more refined extrapolation.

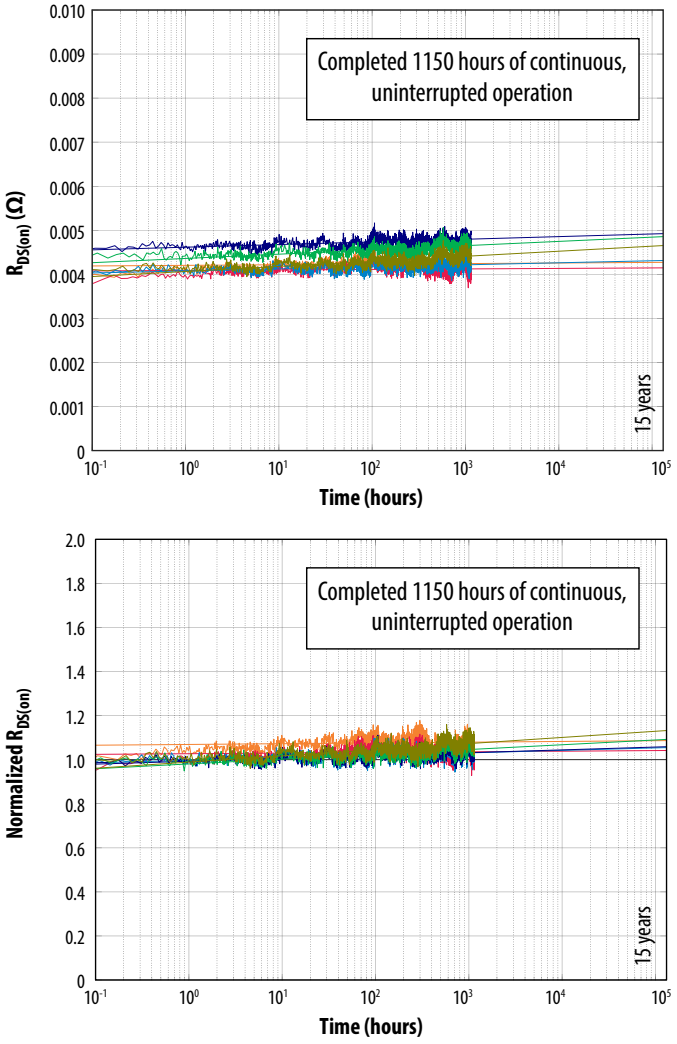


Figure 15: Long-term dynamic $R_{DS(on)}$ for six samples of EPC2218 eGaN FETs under continuous resistive hard-switching operation for over 1000 hours at ambient temperature and a bias of 100 V. The graph on the top shows $R_{DS(on)}$ versus Time, while the bottom graph shows $R_{DS(on)}$ normalized to its value after the first 10 minutes. Note that even over 1000 hours of operation, $R_{DS(on)}$ does not deviate from a simple log(time) growth dependence.

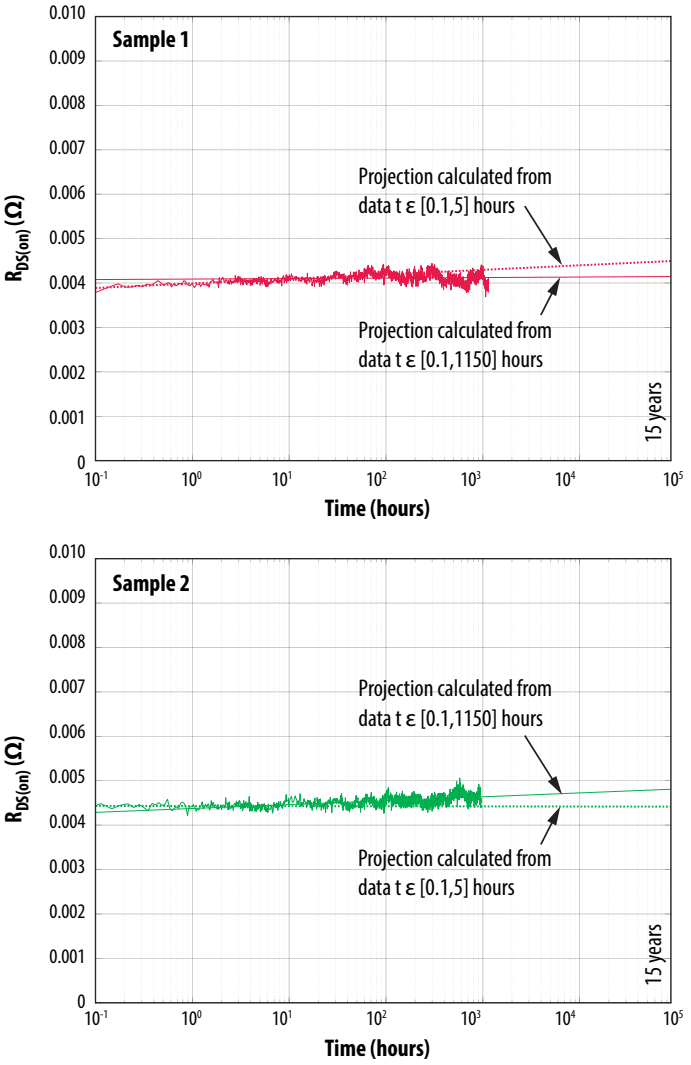


Figure 16: Comparison of log(time) fits to the $R_{DS(on)}$ data, where the dashed line represents the fit over the first 5 hours, while the solid line represent the fit over the full 1150 hours. Data for two samples of EPC2218 are shown. Note that the short-term fit has a similar projection to the long-term fit, with small random differences of ± 10% on the 15 year projection.

2.2 Inductive vs. Resistive Hard Switching and the Effect of Switch Current

Designers have raised concerns that resistive hard switching is not truly representative of the kind of hot-carrier stress that occurs during inductive hard switching. These concerns have also been voiced in the academic literature, at conference proceedings, and by other GaN manufacturers. The argument centers on the loci the part traverses in current-voltage space during an on-transition. For an inductive transition, the FET experiences higher current during the critical interval of time when both voltage and current are high, precisely the conditions that lead to hot-carrier effects. Though plausible, these arguments are mostly hand-waving, and are never supported by hard data or solid theory.

To address this question, both inductive and resistive hard switching conditions were measured. The measurement system was able to alternate from inductive to resistive modes (and back) on the same device under test. For inductive mode, the test circuit is a boost converter operating in Continuous Conduction Mode (CCM). In both modes, the part is switching continuously at 200 kHz, and oscilloscope traces are captured periodically, allowing monitoring of both short term and long term dynamic $R_{DS(on)}$.

Figure 17 shows data for an EPC2204 GaN transistor switching at 80 V. For the first four hours, the part was operated in inductive mode. After that, it was operated in resistive mode for the ensuing four hours. To guarantee a fair comparison, the off-state voltage across the device, frequency, duty cycle, and current at turn-on were kept the same for the resistive and inductive cases. As can be seen in the figure, there is no discernable difference in the slope or intercept of the log(t) growth characteristic: resistive and inductive hard-switching are essentially indistinguishable in terms of dynamic $R_{DS(on)}$. The same is true of short-term effects within the first microsecond of the transition; for neither mode displayed any "fast" recovery effects.

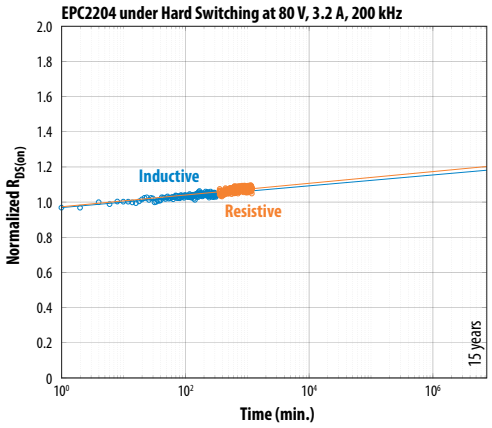


Figure 17: Comparison of inductive versus resistive hard switching on an EPC2204 FET switching at 80 V, 200 kHz. The same part was tested under inductive mode for the first four hours, followed by resistive mode for the next four hours. Both modes are essentially indistinguishable in terms of dynamic $R_{DS(on)}$.

This result implies that the mechanism responsible for $R_{DS(on)}$ shifts in GaN transistors is either independent, or weakly dependent on the detailed loci of current-voltage traversed during a transition. In both switching cases, there is simultaneous voltage and current during turn-on. While in resistive switching, the voltage across the transistor decreases as the current rises; whereas, in a purely inductive turn-on, the current rises before the voltage collapses. The fact that dynamic $R_{DS(on)}$ is so similar between the modes suggests that the electron current has a weak influence on hot-carrier trapping.

To explore this hypothesis more, resistive hard-switching measurements on an EPC2206 device at two different switch currents was conducted. Figure 18 (top) shows the results. One part was tested at 12.8 A and another was tested at 25.6 A, double the switch current. To account for the distinct device heating in each case, $R_{DS(on)}$ is normalized to its value at 10 minutes. Here, as before, the switching current has no discernible effect on either the slope or intercept of the log(t) growth characteristic. Similarly, the effect of switch current on the slope was evaluated under inductive hard switching.

Figure 18 (bottom) shows the EPC2204 device operated in a buck converter at different currents and 80 V output voltage. Starting with 1 A switch current for the first 1.5 hours, followed 3.5 hours with 5 A, and finishing with 10 A for 20 additional hours. For an easier interpretation of the results, the $R_{DS(on)}$ measurements were normalized to the thermal steady state $R_{DS(on)}$ at the beginning of each interval.

As discussed below, the physics-based model of dynamic $R_{DS(on)}$ explains the results above. This model predicts that switch current (or the switching loci) has no impact on slope of the log(t) growth line, as observed. Furthermore, the model predicts that switch current does affect the intercept of the line, but only weakly. In fact, the intercept (or additive vertical offset) of the line will increase like the logarithm of the switch current. For the same reason, the fine details of the switching loci have almost no impact, and inductive and resistive hard switching are equally valid methods to characterize dynamic $R_{DS(on)}$.

While equally valid to an inductive test circuit, a resistive circuit presents several practical advantages when it comes to evaluating dynamic $R_{DS(on)}$. For one, the circuit is simpler and more compact, allowing it to be integrated on probe cards for wafer-level characterization. For another, the lack of voltage overshoot during turn off allows for testing at voltages closer to the breakdown voltage, achieving operating points in the switching loci even more severe than possible with an inductive switching circuit.

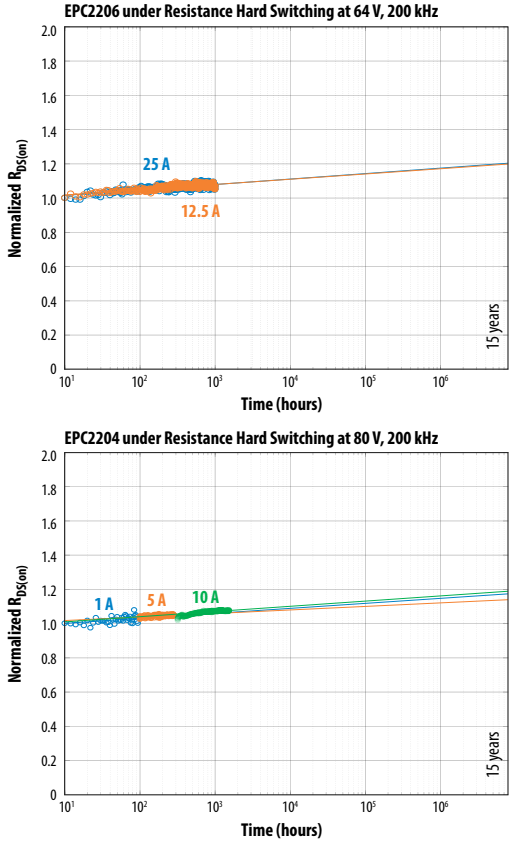


Figure 18: Effect of switch current on dynamic $R_{DS(on)}$. (top) Two EPC2206 devices were tested under resistive hard switching at 64 V, 200 kHz. (bottom) The same device was tested under inductive hard switching and three different currents at 80 V, 200 kHz. No discernible difference was found in the slope or intercept of the log(t) growth characteristics.

2.3 Alternating Hot/Cold Switching Test

Additional hard-switching reliability tests were performed at lower temperatures than reported previously [22]. Using a specially designed thermoelectric module attached to the backside (case) of the device under test, it was possible to achieve temperatures as low as –30°C while the part is switching. (Note that this condition is academic in nature; even in very cold ambient conditions, the device would not stay at this low temperature owing to self-heating).

A typical result is shown in Figure 19, where an EPC2059 device was operated under continuous hard switching while the case temperature was modulated between 80°C and –30°C for two complete cycles. As can be seen, when the temperature drops to –30°C, $R_{DS(on)}$ drops as well, owing to increased channel mobility. However, it begins to rise in time following a log(t) growth characteristic with a distinctly higher slope than it had at 80°C. As the temperature is cycled again, $R_{DS(on)}$ ratchets back and forth between these two distinct lines.

These data provide even more evidence that the slope of the log(t) growth law has a negative temperature coefficient, which is explained in the model to follow. Though the slope is indeed higher at –30°C (close to datasheet minimum of –40°C), even if the part were operated non-stop for 10 years in this unrealistic condition, $R_{DS(on)}$ would still be lower than had it operated at 80°C for the same time.

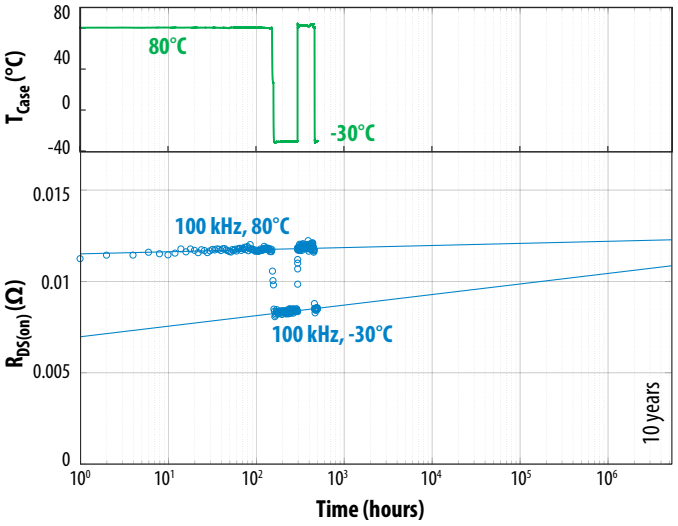


Figure 19: Effect of alternating hot-cold conditions on dynamic $R_{DS(on)}$ for an EPC2059. (Top) Case temperature versus Time, as controlled by a thermoelectric cooler. (Bottom) $R_{DS(on)}$ versus Time. Switching is continuous throughout at 100 V and 100 kHz.

2.4 Physics-Based Dynamic $R_{DS(on)}$ and Lifetime Models

EPC has developed a first-principles mathematical model to describe the dynamic $R_{DS(on)}$ effect in eGaN FETs from the basic physics of hot carrier scattering into surface traps. The model successfully predicts all of the following phenomena:

- $R_{DS(on)}$ growth with time
- The slope of $R_{DS(on)}$ over time has a negative temperature coefficient (i.e., lower slope at higher temperature)
- Switching frequency does not affect the slope, but causes a small vertical offset
- Switching current does not affect the slope
- Negligible difference between inductive and resistive hard switching

2.5 Physics-Based Dynamic $R_{DS(on)}$ Models

The model is predicated on the assumption that hot electrons inject over a surface potential into the conduction band of the surface dielectric. Once inside, the electrons quickly fall into deep mid-gap states, where they are assumed to be trapped permanently (no de-trapping). Hot electrons are created during the switching transition, where the transient combination of high injection current and high electric field leads to a significant number of high energy carriers.

Figure 20 shows a cross-section of an GaN transistor in the immediate vicinity of the drain contact. During a hard-switching transition, electrons rush toward the drain, and become highly accelerated by the electric fields there. Under the right conditions, some electrons gain sufficient kinetic energy to scatter into the conduction band of the dielectric above. To do so, they need kinetic energy > 2 eV. Once inside the dielectric, they trap in deep mid-gap states, and become permanently trapped. When the device is turned on, the trapped charge reduces the normal channel electron charge, leading to a rise in $R_{DS(on)}$. By expanding on this simple dynamical picture of charge trapping in the discussion to follow, a model is derived that explains all the observed characteristics above.

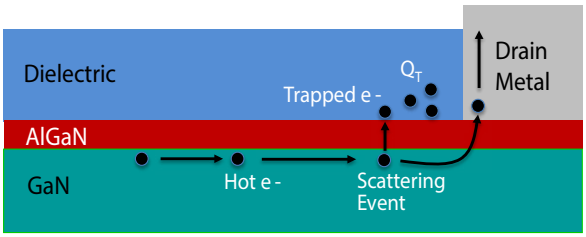


Figure 20: Schematic diagram showing hot electron scattering into the surface dielectric near the drain contact. To enter this dielectric, electrons must have sufficient energy to surmount the potential barrier. Once in this dielectric, they fall into deep electron trap states and are trapped effectively indefinitely.

2.5.1 Key Assumptions

The hot electron energies follow an exponential (Maxwellian) distribution at the high energy tails.

- The hot electron energies follow an exponential (Maxwellian) distribution at the high energy tails.
- Hot electrons become trapped in the surface dielectric near the drain contact via a two-step process:
  - Scattering and ballistic transport over the surface potential barrier into the conduction band of the dielectric

Subsequent trapping in deep electron gap states within the dielectric

- To enter the dielectric, hot electrons need sufficient energy to surmount the surface potential barrier (conduction band offset + built-in field). Tunneling is ignored.
- Only electron trapping near the drain is considered (although this theory would extend equally well to other locations within the drift region).
  - Trapping near the gate can occur also, leading to V_{TH} shifts and an increase in $R_{DS(on)}$. However, gate side trapping is of minor practical concern in eGaN technology.
- Once electrons enter the dielectric, they become trapped near the surface, contributing to a growing surface trapped charge density denoted by Q_S.
  - Q_S is modeled as a surface charge density, ignoring its distribution along the z-axis
- Once electrons are trapped, they never leave (no de-trapping or recovery in time).
  - This is a conservative assumption leading to a worst-case dynamic $R_{DS(on)}$ growth.

2.5.2 Hot Electron Energy Distirbution

Hot electron effects in AlGaN/GaN HEMTs have been studied extensively both experimentally and from first principles theoretical computations [23–27]. Hot electrons emit light (electroluminescence) with a spectrum characteristic of their energy distribution. By measuring the spectrum, Brazzini et al. [28] was able to experimentally measure the hot carrier energy distribution in a HEMT under different bias states. This study found that the hot carrier distribution in the high energy regime tails is well fit by an exponential (Maxwell-Boltzman distribution) with a characteristic electron temperature T_e (2000 K) well above the lattice temperature. However, these authors did not provide a straightforward way to model the electron temperature versus the electric field or lattice temperature.

For the purposes of this development, an analytical expression for the hot carrier temperature is unnecessary. It is sufficient to know that at high energies, the fraction of carriers decreases exponentially with energy. Meneghini et al. [29], based on the lucky-electron model of Hu et al. [30], proposed that the faction of high energy carriers over energy range scales with electric field as:

$$f(E)dE \propto Ee^{-E/qF\lambda}dE \qquad \text{Eq. 9}$$

where *E* is the electron energy (above the conduction band minimum), *F* is the electric field, and λ is the electron mean free path between scattering events. The term in the denominator of the exponential represents the energy gained by an electron from the electric field over a mean free path. We adopt this formalism in the analysis to follow.

2.5.3 Surface Trapping Rate Equation

The top portion of Figure 18 provides a schematic band diagram showing band alignment vertically near the drain contact. A surface barrier exists for electrons to enter the conduction band of the Si_3N_4 surface dielectric. The overwhelming majority of channel electrons have insufficient kinetic energy to surmount the barrier. But a small percentage of hot electrons do gain sufficient energy and become trapped in the dielectric via a three-step process: (1) gain enough kinetic energy from the field in the channel to surmount the surface barrier (2) scatter and travel ballistically across the AlGaN front barrier into the conduction band of the Si_3N_4 (3) fall into deep mid-bandgap trap states in the insulator.

The bottom portion of Figure 21 shows the same situation, but now the surface electrostatic barrier (red dashed lines) has been enhanced by the trapped surface charge Q_s. This increase in the barrier makes it exponentially more unlikely for electrons to scatter into the Si_3N_4. As we will see shortly, this dynamic leads to a rapidly self-quenching charge trapping rate, resulting in the (slow) logarithmic growth of $R_{DS(on)}$ in time.

The trapping rate is proportional to the number of hot electrons with energy sufficient to cross the surface potential barrier. This number can be calculated by integrating the hot-carrier distribution for all energies above the barrier height. The barrier height will consist of two contributions: (1) a constant built-in barrier, Φ_{bi}, and (2) a dynamically changing component due to the electrostatics of the trapped surface charge. We denote this dynamic component by β x Q_S, where β is merely a geometric (electro-static) factor relating Q_S to the change in barrier height.

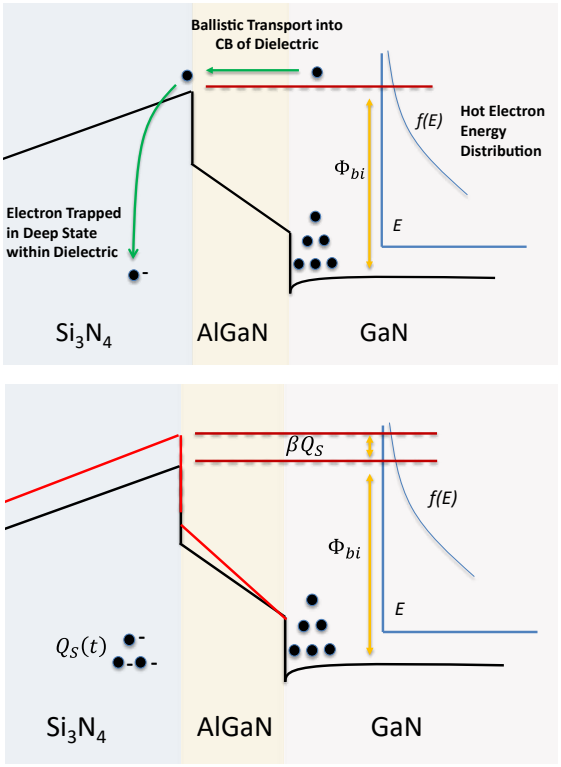


Figure 21: (Top) Emission over a surface barrier. Schematic band diagram showing band alignment vertically near the drain contact. A surface barrier exists for electrons to enter the conduction band of the Si_3N_4 surface dielectric. The overwhelming majority of channel electrons have insufficient kinetic energy to surmount the barrier. But a small percentage of hot electrons do have the energy and enter the insulator via a three-step process described in the text. (Bottom) Surface electrostatic barrier has now been enhanced by Qs, as depicted by dashed red lines.

Carrying out this integral, we find that:

$$\frac{dQ_S}{dt} = A\int_{\Phi_{bi}+\beta Q_S}^{\infty} f(E)dE = A\int_{\Phi_{bi}+\beta Q_S}^{\infty} Ee^{-E/qF\lambda}dE$$
$$\approx A\Phi_{bi}e^{-(\Phi_{bi}+\beta Q_S)/qF\lambda} \equiv B\, e^{-\beta Q_S/qF\lambda} \qquad \text{Eq. 10}$$

This approach leads to the fundamental surface charge rate differential equation:

$$\frac{dQ_S}{dt} = B\exp\left(-\frac{\beta Q_S}{qF\lambda}\right) \qquad \text{Eq. 11}$$

where we have lumped some temperature and electric-field dependence into the parameter *B*. Note also that the pre-factor *B* will increase linearly with current and switching frequency.

The solution to this differential equation is:

$$Q_S(t) = \frac{qF\lambda}{\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right) \qquad \text{Eq. 12}$$

Here we have obtained a fundamental result that the trapped surface charge grows with log(t). This will reverberate thru the development to follow and is the basis of the observed log(t) growth characteristic in $R_{DS(on)}$.

2.5.4 Impact on $R_{DS(on)}$

At this point, we have found an expression for the trapped charge $Q_S(t)$ in the surface dielectric near the drain vs time. This surface charge causes in increase in the channel resistance of the device when the drain bias has been removed and the device is in the on-state. To first order, the surface charge will lead to a commensurate decrease in the 2DEG channel charge density. If we denote Q_P the normal (piezoelectrically induced) electron density for a virgin device, we can calculate the total device resistance via:

$$R(t) = R_0 + \frac{C}{Q_P - Q_S} = R_0 + \frac{C}{Q_P - \frac{qF\lambda}{\beta}\log\left(1 + \frac{B\beta}{qF\lambda}t\right)} \quad \text{Eq. 13}$$

In this equation, R_0 represents the resistance of the device away from the drain region, including channel and drift resistance. The second term represents resistance from the immediate vicinity of the drain where the channel 2DEG density Q_P has been reduced via the trapped surface charge Q_S, where C is a constant relating this resistance to charge. The value of C will change with temperature, e.g., due to the access region mobility, but this temperature dependence will cancel out during normalization later.

For typical operating conditions, surface charge injection will remain small in comparison to the built in 2DEG piezoelectric charge ($Q_S << Q_P$). In this regime, it is appropriate to use the Taylor expansion 1/(1-x) = 1 + x to simplify Equation 13 further:

$$R(t) \approx R_0 + \frac{C}{Q_P}\left[1 + \frac{qF\lambda}{Q_P\beta}\log\left(1 + \frac{B\beta}{qF\lambda}t\right)\right] \quad \text{Eq. 14}$$

2.5.5 Temperature Dependence

For temperatures > 250 K, high field electron transport in AlGaN/GaN HEMT is dominated by longitudinal-optical (LO) phonon scattering. In GaN, the LO-phonon energy $\hbar\omega_{LO}$ is around 92 meV based on first-principles band structure type calculations [31]. The momentum relaxation time (or scattering time) under LO-phonon scattering will vary with temperature as:

$$\tau_{LO} \propto exp\left(\frac{\hbar\omega_{LO}}{kT}\right) \quad \text{Eq. 15}$$

The temperature dependence of the mean free path can be therefore modeled as:

$$\lambda = v_{th}\tau_{LO} \propto A\sqrt{kT}exp\left(\frac{\hbar\omega_{LO}}{kT}\right) \quad \text{Eq. 16}$$

Note that the mean free path increases as temperature is reduced, because electrons can travel farther between phonon collisions.

Substituting Equation 16 into Equation 14, and re-arranging slightly to calculate fractional change in $R_{DS(on)}$, we obtain:

$$\frac{\Delta R}{R} = \frac{R(t) - R(0)}{R(0)} \approx a + bF\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\sqrt{T}\log(t) \quad \text{Eq.17}$$

In Equation 17 several constants are subsumed into parameters *a* and *b* in order to simplify the notation, but the explicit temperature and field dependence of the model has been retained. Note that the long-time approximation has been used, allowing the additive constant inside the logarithm to be neglected to end up with a simple log(t) time dependence.

2.5.6 Dependence of E-field on Drain Voltage

To make a practical model of $R_{DS(on)}$ growth, there remains one last task, which is to relate the electric field F near the drain contact to the (off-state) drain bias V_{DS} just before the switching transition. In general, this relationship is very complicated, involving a host of design parameters and semiconductor device physics to model accurately. Typically, finite element simulations are employed to tackle this task, and the results do not lend themselves to a practical user equation.

At low drain biases, the 2DEG has not depleted near the drain contact, causing there to be no channel electric field. As V_{DS} increases, the 2DEG eventually depletes all the way to the drain contact, after which the E-field rises linearly with increased V_{DS}. A simple two parameter equation which captures this qualitative behavior is:

$$F \propto \alpha * \ln\left[1 + \exp\left(\frac{V_{DS} - V_{FD}}{\alpha}\right)\right] \quad \text{Eq. 18}$$

V_{FD} is a device dependent offset parameter corresponding to the voltage at which the 2DEG has fully depleted to the drain contact. Roughly speaking, this value is close to the datasheet V_{DSmax} rating for the FET (i.e., V_{FD} = 100 V for 100 V products like EPC2045 or EPC2053). The parameter α is a sharpness (or curvature) parameter, representing how quickly the E-field grows after full depletion. Equation 18 is plotted in Figure 22 for the case of EPC2045.

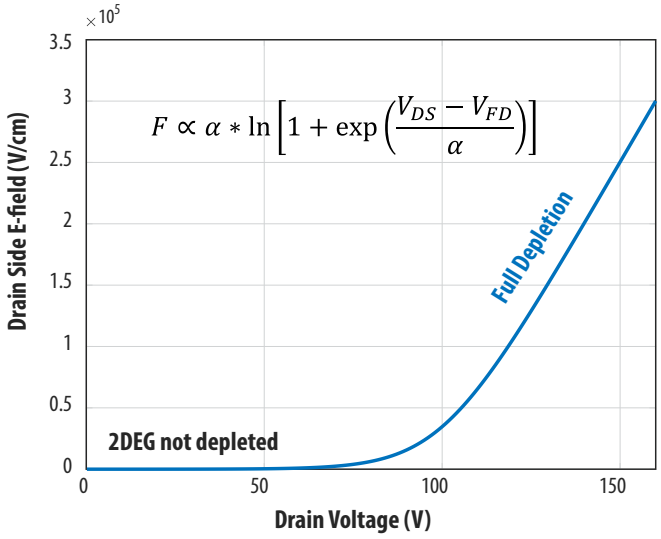


Figure 22: Simple mathematical model for the drain-side E-field versus drain voltage. The E-field smoothly transitions from constant (zero) to a linear regime with an onset voltage corresponding to full depletion of the 2DEG at the drain contact. The parameters V_{FD} and α are device dependent; the values chosen here apply to EPC2045 and related 5th Generation FETs.

2.5.7 Final $R_{DS(on)}$ and Lifetime Equations

Substituting the expression for *F* from Equation 18 into Equation 17 results in the final mathematical model for $R_{DS(on)}$ growth as a function of time, temperature, and drain voltage :

$$\frac{\Delta R}{R} = a + b\log\left(1+\exp\left(\frac{V_{DS}-V_{FD}}{\alpha}\right)\right)\sqrt{T}\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\log(t) \qquad \text{Eq. 19}$$

Independent Variables:

V_{DS} = Drain voltage (V)
T = Device temperature (K)
t = Time (min)

Parameters:

a = 0.00 (unitless)
b = 2.0E-5 ($K^{-1/2}$)
$\hbar\omega_{LO}$ = 92 meV
V_{FD} = 100 V (appropriate for Gen5 100 V products only)
α = 10 (V)

As shown above, the model has three independent variables, and five (device dependent) parameters. Note that time must be inserted in units of minutes. The dominant LO-phonon energy for GaN (92 meV) was taken from first principles calculations [29] and is not expected to vary with different GaN transistors. The remaining four parameters were fit to hard-switching dynamic $R_{DS(on)}$ data from EPC2045 over a range of temperatures and drain bias. This parameter set is also directly applicable to the following 5th Generation 100 V GaN transistors: EPC2053, EPC2218, and EPC2204. In general, some parameters may vary for devices from different product families. Please consult EPC for parameter values appropriate to other eGaN products.

Many customers require lifetime estimates under specific use conditions to fulfill certain quality or reliability requirements. By defining the lifetime (under hard-switching conditions) as the time <*t*> at which $R_{DS(on)}$ will rise 20% from its initial value, Equation 20 can be inverted in a straightforward manner to obtain:

$$\langle t\rangle = \exp\left[\frac{(0.2-a)}{b\log\left(1+\exp\left(\frac{V_{DS}-V_{FD}}{\alpha}\right)\right)\sqrt{T}\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)}\right](\text{min}) \qquad \text{Eq. 20}$$

This equation gives the expected MTTF under hard-switching conditions as a function of operating voltage and temperature. Typically, worst case values (highest voltage, lowest temperature) are used to provide a lower bound. As before, the lifetime will be in units of minutes. Other definitions of lifetime can be applied and extracted from Equation 20 as well.

2.5.8 Effect of Switching Frequency and Switching Current

In the analysis so far, the effects of switching frequency *f* and switch current I on the $R_{DS(on)}$ growth characteristics have been ignored. The current directly impacts the number of electrons injected into the high field region during the hard-switching transition, and therefore has a linear effect on the hot carrier density. Likewise, the switching frequency determines the number of hot carrier pulses seen at the drain in a given time interval, and therefore also has a linear effect on the surface trapping rate.

In our surface trapping rate Equation 11, the effects of frequency and switch current are subsumed into the constant *B*. If we make the intuitive assumption that *B* is linearly proportional to both *f* and *I*, and carry the math through to our final expression in Equation 17, we derive a simple scaling result that relates the $R_{DS(on)}$ growth in one switching condition (f_1,I_1) to that in another (f_2,I_2):

$$R(t;f_2,I_2) = R(t;f_1,I_1) + b\left(\log\left(\frac{f_2}{f_1}\right)+\log\left(\frac{I_2}{I_1}\right)\right) \qquad \text{Eq. 21}$$

Mathematically, the effect of changing the switching frequency or current is to simply offset the $R_{DS(on)}$ growth curve vertically by a small amount. The offset depends on the logarithm of f and I, and therefore has a fundamentally weak dependence on these variables. Furthermore, the offset depends on the overall slope *b* of the log(t) growth characteristic. Therefore, if the FET is operated under conditions with low $R_{DS(on)}$ rise (low slope *b*), the effect of changing frequency or current will be negligible.

Figure 23 compares the modeled $R_{DS(on)}$ vs. time for an EPC2045 at three different switching frequencies, from 10 kHz to 1 MHz. Note that the curves are simply offset from each other vertically. The same would be true had we compared different switch currents. Because the offset changes as the logarithm of *f* (or *I*), even a 10x increase in switching frequency (or current) would be difficult to observe experimentally owing to ±10% noise in the measurement and projection.

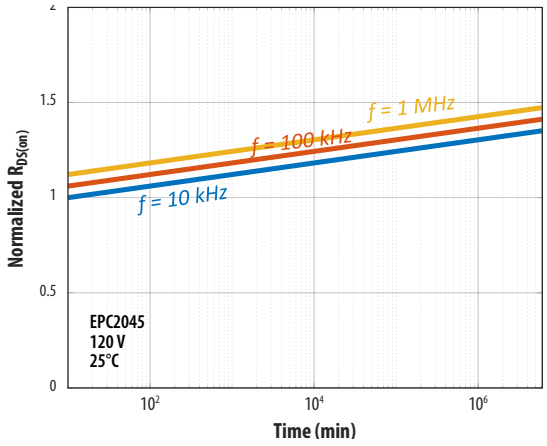


Figure 23: Modeled $R_{DS(on)}$ vs. Time at three different switching frequencies, covering two orders of magnitude. Note that the effect of frequency change is a small vertical offset in the growth characteristic. The same offset would occur at different switch currents.

The logarithmic scaling relationship explains several of the experimental results discussed earlier. In the measurements of EPC2206 at two different switch currents in Figure 18, even a 2x increase in the switching current did not register as a perceptible change in the $R_{DS(on)}$ growth curves. In the comparison of resistive versus inductive hard-switching, the locus of current-voltage points traversed during the transition is thought to be more punishing in the case of inductive switching. This assumption is discussed at length in the academic literature [32], and is often invoked as an argument (without evidence) against the use of resistive hard-switching to characterize GaN HEMTs. However, the weak (logarithmic) dependence of $R_{DS(on)}$ on switch current explains why we observed no significant differences when we compared inductive and resistive hard-switching on the same device. Given this combination of data and theory to back it up, EPC will continue using the simpler and more accurate resistive hard-switching test method to characterize GaN devices.

2.5.9 Impact of Higher Stress Voltages

In the case where the amount of trapped charge approaches the number of electrons available in the 2DEG (Q_S approaches Q_P), the simplifying assumption used in Equation 13 to get to Equation 14 is no longer valid. This situation could occur when devices are taken to voltages well above their design limits. In Figure 24 are shown EPC2045 devices tested up to 150 V at 75°C and 125°C. Note how the straight-line extrapolation that would occur with a simple log(time) dependence is no longer applicable. If the simplifying assumption of small trapped charge is not made, the following result is obtained:

$$\frac{\Delta R}{R} \equiv \frac{R(t)-R(0)}{R(0)} = \frac{C}{Q_P}\left[\frac{\frac{qF\lambda}{\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right)}{Q_P-\frac{qF\lambda}{\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right)}\right] \quad \text{Eq. 22}$$

$$= \frac{C}{Q_P}\left[\frac{\frac{qF\lambda}{Q_P\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right)}{1-\frac{qF\lambda}{Q_P\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right)}\right] \quad \text{Eq. 23}$$

To simplify notation, let $\Psi \equiv \frac{qF\lambda}{\beta}$ Eq. 24

(Please refer to Equation 16 for a definition of λ and Equation 18 for a definition of F)

Then substituting Equation24 into Equation 23

$$\frac{\Delta R}{R} = \frac{C}{Q_P}\left[\frac{\frac{\Psi}{Q_P}\log\left(1+\frac{B}{\Psi}t\right)}{1-\frac{\Psi}{Q_P}\log\left(1+\frac{B}{\Psi}t\right)}\right] \quad \text{Eq. 25}$$

We now obtain the full model equation:

$$\frac{\Delta R}{R} = a_1\left[\frac{a_2\Psi\log(1+a_3t/\Psi)}{1-a_2\Psi\log(1+a_3t/\Psi)}\right]$$

where: $a_1 \equiv \frac{C}{Q_P}$ $a_2 \equiv \frac{1}{Q_P}$ $a_3 \equiv B$ Eq. 26

h the following expanded list of parameters:

- a_1 = 0.6 (unitless)
- a_2 = b/a_1 (where b = 2.0E-5 $K^{-1/2}$ from [28])
- a_3 = 1000 ($K^{1/2}$ min^{-1})
- b = 2.0E-5 ($K^{-1/2}$)
- $\hbar\omega_{L0}$ = 92 meV
- V_{FD} = 100 V (appropriate for Gen5 100 V products only)
- α = 10 (V)
- T = Device temperature (K)
- t = Time (min)

Calculating Equation 26 using the expanded list of parameters yields the solid lines in Figure 24, giving further evidence of the validity and applicability of this physics-based model.

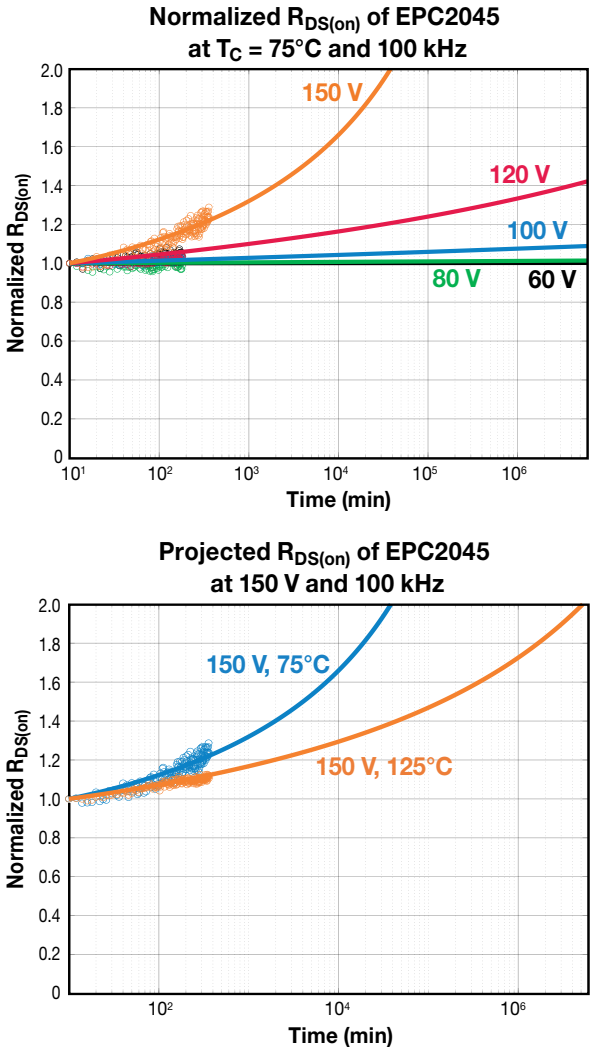


Figure 24: 100 V EPC2045 devices in hard-switching circuit at various voltages up to 150% of design rating (top), and at two different temperatures, also at 150% of design rating (bottom). The solid lines are the model predictions, and the dots represent measurement point.

2.5.10 200 V Model

A similar analysis was developed for 200 V GaN transistors. The resultant variables are as follows:

- a_1 = 0.6 (unitless)
- a_2 = $2.8 \cdot b/a_1$ (where b = 2.0E-5 $K^{-1/2}$ from [28])
- a_3 = 1000 ($K^{1/2}$ min^{-1})
- b = 2.0E-5 ($K^{-1/2}$)
- $\hbar\omega_{L0}$ = 92 meV
- V_{FD} = 210 V (appropriate for Gen5 200 V products only)
- α = 25 (V) (appropriate for Gen5 200 V products only)
- T = Device temperature (K)
- t = Time (min)

Figure 25 shows the results from Equation 26 using the variables for 200 V devices. These calculated results are then compared against actual measurements. On the left is the normalized $R_{DS(on)}$ for the fifth-generation, 200 V rated EPC2215 at three voltages. The highest voltage, 280 V, is 40% above the maximum rating. On the right are measurements compared with the model at two different temperature and at the maximum rated voltage.

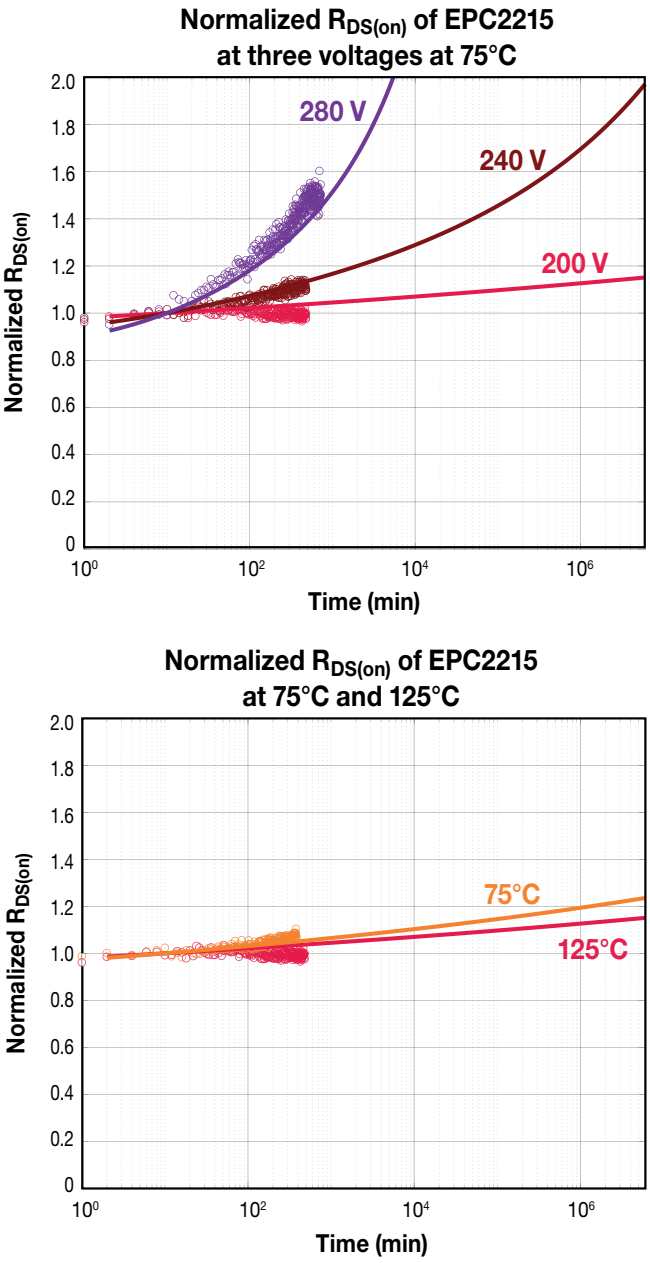


Figure 25: (top) 200 V EPC2215 normalized $R_{DS(on)}$ at three voltages. Note that 280 V is 40% above the maximum rated voltage (bottom). EPC2215 at 75°C and 125°C and 200 V. The solid lines are the results from Equation 20 using variables for 200 V devices, and the dots are actual measurements.

2.5.11 Conclusions for Physics-Based Dynamic $R_{DS(on)}$ Model

EPC has developed a first principles physics-based model to explain $R_{DS(on)}$ rise in GaN transistors under hard-switching conditions. The model is predicated on the assumption that hot electrons inject over a surface potential into the conduction band of the surface dielectric. Once inside, the electrons quickly fall into deep mid-gap states, where they are assumed to be trapped permanently (no de-trapping). Hot electrons are created during the switching transition, where the transient combination of high injection current and high fields leads to a hot carrier energy distribution with long tails into the high energy regime.

This model predicts the following observations:

- $R_{DS(on)}$ growth with time
- The slope of $R_{DS(on)}$ over time has a negative temperature coefficient (i.e., lower slope as temperature rises).
- Switching frequency does not affect the slope but causes a small vertical offset.
- Switching current does not affect the slope.

The time dependence results from a rapidly self-quenching charge trapping dynamic that involves two inter-twined effects: (1) a hot electron energy distribution that is exponential in energy; and (2) an accumulating surface charge Q_S that steadily raises the barrier for electron injection into the dielectric. The combination of these effects leads to a trapping rate that becomes exponentially slower as charge accumulates, leading to a slow time dependence. As the number of trapped charges approaches the number of available electrons in the 2DEG, the $R_{DS(on)}$ appears to climb faster than a straight log(time) dependence. The trapping mechanism, however, continues to follow a true log(time) dependence.

The negative temperature dependence results from the effect of LO-phonon scattering on the hot carrier energy distribution. At lower temperature, decreased scattering improves the mean free path, allowing electrons to gain higher energy in an electric field.

Key parameters in the mathematical model were fit to measured results for the EPC2045 across a range of drain voltages and temperatures. The model allows users to project long-term $R_{DS(on)}$ growth as a function of four key input variables: drain voltage, temperature, switching frequency, and switching current. The model was adapted to provide a simple MTTF equation, allowing users to predict lifetime under arbitrary conditions.

SECTION 3: APPLYING THE MODEL TO COMMON REAL-WORLD USE CASES

In this section, we apply the model to some common real-world use cases: (i) a synchronous rectifier and (ii) a buck converter, considering both the high side and low side FETs. For these calculations, we used a two-step simulation process.

In the first step, we developed realistic SPICE models of the application circuits, including the effects of key parasitic inductances that occur in practical layouts. These parasitics have a first-order effect on ringing and voltage overshoot and can therefore impact dynamic $R_{DS(on)}$ in the FET itself. Parasitic inductances were varied from typical all the way to extreme (representative of very poor PCB layout). The SPICE simulations captured the channel current and drain-source voltage inside the FET with fine time sampling throughout a single switching cycle.

In the second step, these single-cycle current-voltage loci were imported into the hot electron trapping model (implemented in MATLAB). Using this model, we calculate the charge trapping that occurs in the very first switching cycle, and determine at what times (e.g., turn-on or turn-off transitions) the most charging occurs. Furthermore, we can integrate over trillions of identical switching cycles to determine the cumulative charge trapping that would occur over 10 years of continuous operation. Because the instantaneous trapping rate depends (non-linearly) on the cumulative trapped charge, the amount of charging per cycle is not constant, but instead rapidly self-quenches over time as the FET switches. Not only does the charging saturate in time, but the regions within a switching waveform that are most detrimental can also change as the device operates. Take for example the case of the hard-switch high-side FET in a buck converter (to be discussed in detail later). Initially, charge trapping occurs predominantly during the high-current/moderate voltage loci at the turn-on transition. However, after long-term operation, this process quenches completely, and all further charging occurs only during the low-current/high voltage loci of the turn-off transition.

The following conclusions will be supported by these calculations:

For a 48 V–12 V LLC Synchronous rectifier:

Under these zero-voltage switching (ZVS) conditions, dynamic $R_{DS(on)}$ ($dR_{DS(on)}$) is generally very benign.

- Users can consider using 30 V transistor in lieu of conservative 40 V transistor with a 12 V output and 24 V bus voltage.

For a Low Side FET in Buck Converter (Soft switching) using latest-generation 100 V GaN devices:

Benign $dR_{DS(on)}$, even with 50 V overshoot on an 80 V bus voltage for the turn on transition.

- Extreme overshoot to 170 V can lead to appreciable $dR_{DS(on)}$

For a High Side FET in Buck Converter (Hard switching) using latest-generation 100 V GaN devices:

- Under moderate overshoot of 40 V (130 V peak), charge trapping occurs predominantly during the turn on transition, and long-term $dR_{DS(on)}$ is benign.
- Under extreme overshoot of 90 V (170 V peak), charge trapping is dominated by the high voltage ringing following the turn-off transition, and long-term $dR_{DS(on)}$ could be a concern.

3.1 Current-Dependent Hot Electron Trapping Model

To simulate dynamic charge trapping within individual switching cycles, we made two simple generalizations to the basic governing differential equation (Equation 11) discussed previously. For one, we assumed that the instantaneous trapping rate is linearly proportional to the channel current (I). From a device physics perspective, this reasonable assumption is tantamount to saying the channel electrons act independently (non-interacting), and each has an equal probability of becoming a "lucky" electron with sufficient kinetic energy to surmount the surface barrier and become trapped. Note that the drain-side electric field F dependence on V_{DS}, and the junction temperature dependence of the mean free path λ, were captured in Equations 18 and 16 and are repeated here for convenience.

$$\frac{dQ_S}{dt} = B \exp\left(-\frac{\beta Q_S}{qF\lambda}\right) \quad \text{Eq.11}$$

where

$$F \propto \alpha * \ln\left[1 + \exp\left(\frac{V_{DS} - V_{FD}}{\alpha}\right)\right] \quad \text{Eq. 18}$$

$$\lambda = v_{th}\tau_{LO} \propto A\sqrt{kT}exp\left(\frac{\hbar\omega_{LO}}{kT}\right) \quad \text{Eq. 16}$$

The second generalization relates to the integration of Equation 11 in time. In our previous analysis, we assumed the current and voltage were not changing in time. This allowed us to immediately integrate Equation 11 to obtain a closed-form analytic solution for the surface charge vs. time (Equation 12). For the more general cases considered here, we have allowed both current and voltage to change in time throughout the loci of a switching cycle. As a result, there is no closed form solution, and we must explicitly integrate Equation 11 in time, leading to the general solution shown in Equation 27 below. This integration must be performed numerically owing to the complexity of the switching waveforms.

$$Q_S(t) = B' \int_0^t I(t)\, exp\left(-\frac{\beta Q_S}{qF(t)\lambda}\right) dt \quad \text{Eq. 27}$$

Equation 27 represents a significant development in the theoretical understanding of dynamic $R_{DS(on)}$ in GaN transistors. Researchers have long known that both the current and voltage are the key drivers of hot electron trapping in these devices. But they have not known how to combine their effects mathematically to compute cumulative trapped charge and dynamic $R_{DS(on)}$. As seen in Equation 27, the effect of current is linear, while the effect of V_{DS} (through the electric field term F) is highly non-linear and depends on the trapped charge Q_S that has already accumulated. For this reason, as the FET switches over longer time scales and Q_S rises, it is only the hottest electrons, resulting from highest field F and highest V_{DS} loci, that can contribute to further trapping. This effect will become clearer as we analyze practical use-cases in the discussion to follow.

The next step is to consider a set of real-world examples. In the first example, a 48 V–12 V LLC synchronous rectifier operating at 1 MHz will be used to evaluate $R_{DS(on)}$ degradation of the secondary side transistors.

3.2 48 V–12 V LLC Synchronous Rectifier

The SPICE model for this circuit is based on the EPC9149 [31] demonstration circuit. The circuit and model parameters are shown in Figure 26. To create different waveforms with more or less overshoot, the leakage inductances L1, L2, L3, and L4 at the output of each of the transformer terminals were varied together from 50 pH to 150 pH. The higher inductance values generated more ringing and overshoot as can be seen in Figure 26 (right).

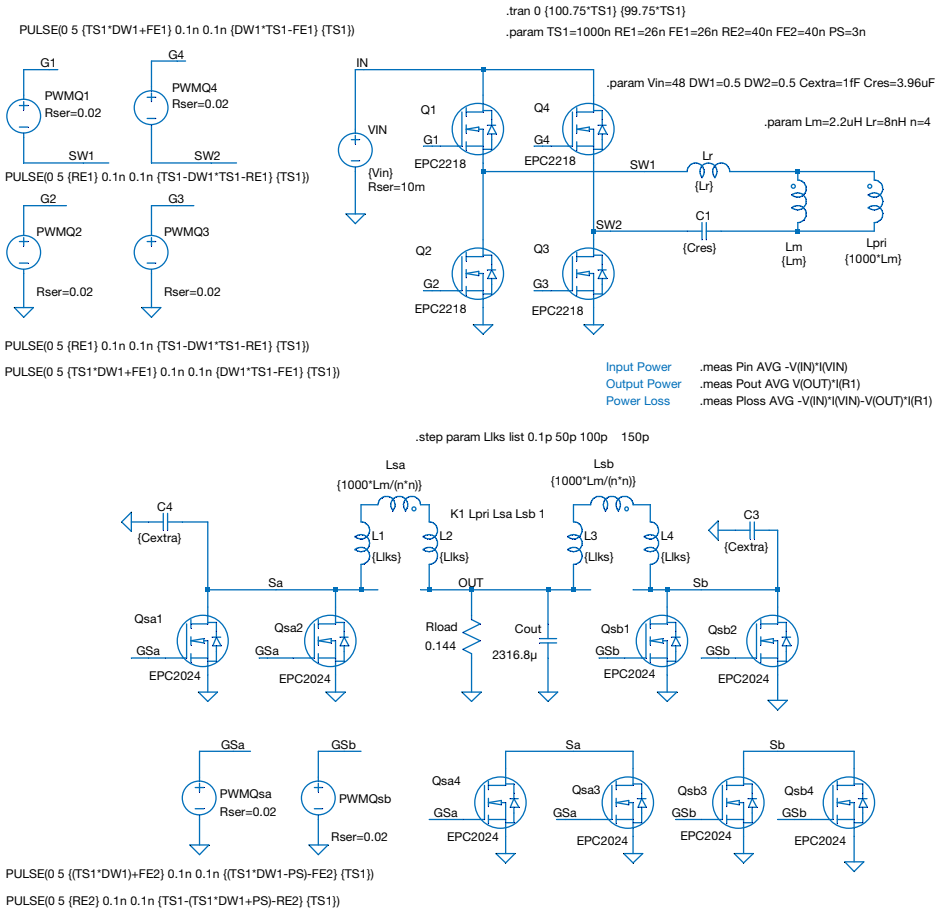


Figure 26: Circuit diagram and SPICE model parameters for a 48 V–12 V LLC synchronous rectifier operating at 1 MHz based on the EPC9149 demo board

Four different cases were studied with the variables being more and less overshoot, and 40 V (case 1 and 2) or 30 V (case 3 and 4) rated GaN devices. In all cases, the eGaN FETs experience a ZVS turn-on and a hard-switched turn-off. The calculations of voltage, current, and $dR_{DS(on)}$ for the entire sequence of switching waveforms from the first cycle to the 10 millionth cycle were made. Figure 27 shows the calculated current and voltage waveforms after 10 million cycles. Throughout each cycle, the amount of trapped charge, Q_S was calculated and summed with all previous cycles.

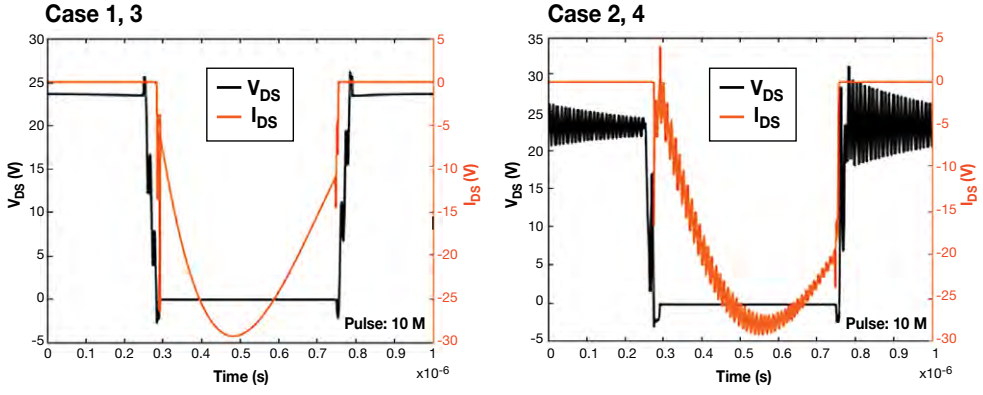


Figure 27: Overshoot was increased in cases 2 and 4 by increasing the inductance values of L1–L4 from 50 pH to 150 pH

3.3 40 V GaN Transistors – Cases 1 and 2

In Figure 28 is shown the results of the calculations using 40 V plotted on a log(t) scale ending at 10 years. In both cases there is no measurable accumulation of trapped charge, and therefore no measurable degradation of $R_{DS(on)}$. In the next two cases, a lower $R_{DS(on)}$ 30 V GaN FET was used. Lower voltage parts typically are more efficient than 40 V parts.

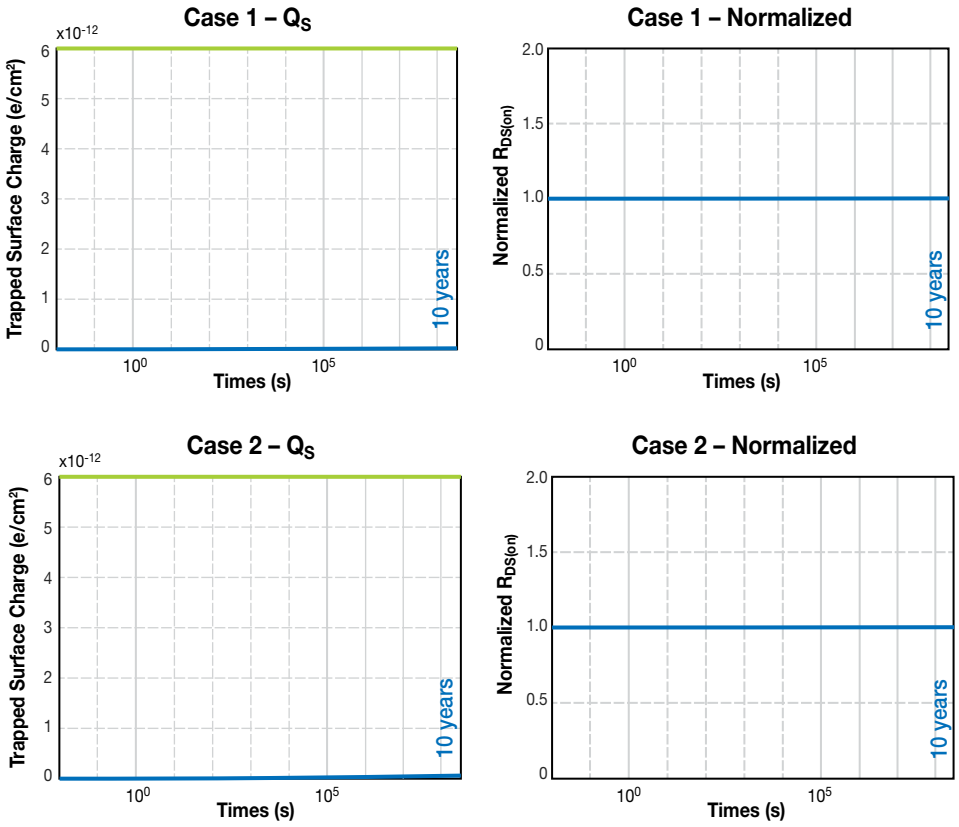


Figure 28: 40 V EPC2024 devices, (upper and lower left) Q_S trapped charge over time, (upper and lower right) normalized $R_{DS(on)}$ over time. Case 1 used L1–L4 = 50 pH, Case 2 used L1–L4 = 150 pH

3.4 30 V GaN Transistors – Cases 3 and 4

In Figure 29 is shown the results of the calculations plotted on a log(t) scale ending at 10 years for the same circuits as used in case 1 and 2, except 30 V EPC2024 GaN transistors were used. In the most extreme case there is about 5%, or minimal degradation of $R_{DS(on)}$. The conclusion is that 30 V devices can safely be used in this circuit, even with the more extreme overshoot.

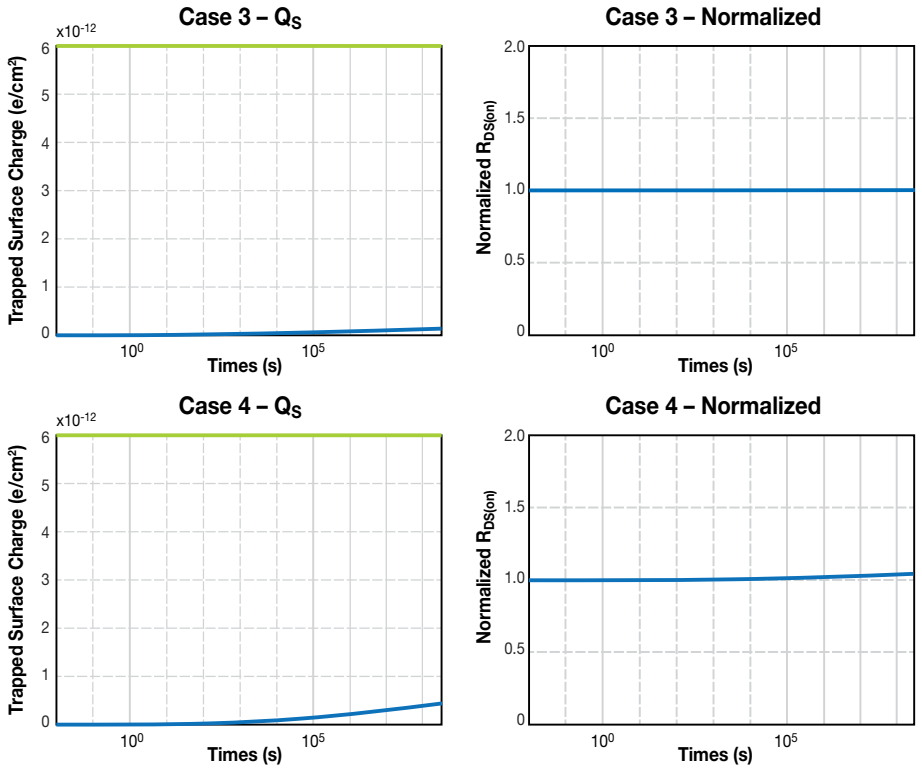


Figure 29: 40 V EPC2024 devices, (upper and lower left) Q_S trapped charge over time, (upper and lower right) normalized $R_{DS(on)}$ over time. Case 1 used L1–L4 = 50 pH, Case 2 used L1–L4 = 150 pH

3.4 48 V–12 V Buck Converter

The next example is for a 48 V–12 V buck converter operating in continuous conduction mode at 500 kHz. The SPICE model circuit schematic is shown in Figure 30. Inductor L5 was varied to modulate the amount of overshoot. The low-side rectifier FET will first be examined, followed by the high-side control FET. Both devices are EPC2045 100 V GaN transistors.

3.5 Low-Side GaN Transistor

Figure 31 shows the voltage and current waveforms of the low-side rectifier FET in the converter with different parasitic inductances. In both cases the low-side transistor experiences soft-switching transients, with increasing voltage overshoot at turn-off as the inductance increases. By varying L5 the overshoot above the 80 V bus went from 50 V to over 90 V peak on the low-side transistor as shown in Figure 31. It should be noted that 170 V peak overshoot is much larger than would be experienced in a well-designed system.

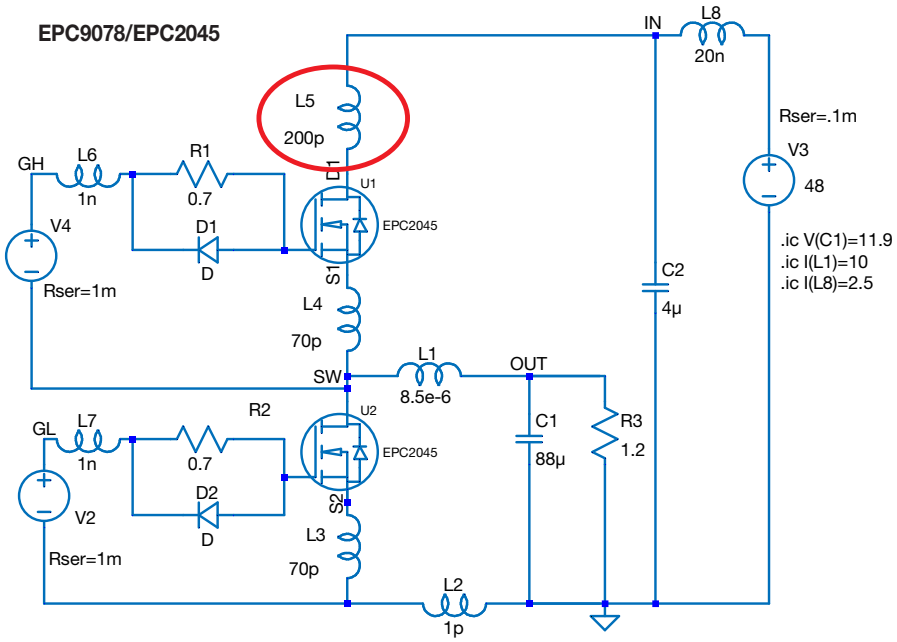


Figure 30: 48 V–12 V buck converter operating at 500 kHz based on EPC9078 demonstration board [32]. To produce different amount of overshoot, L5 was varied from 0.2 nH to 1.2 nH.

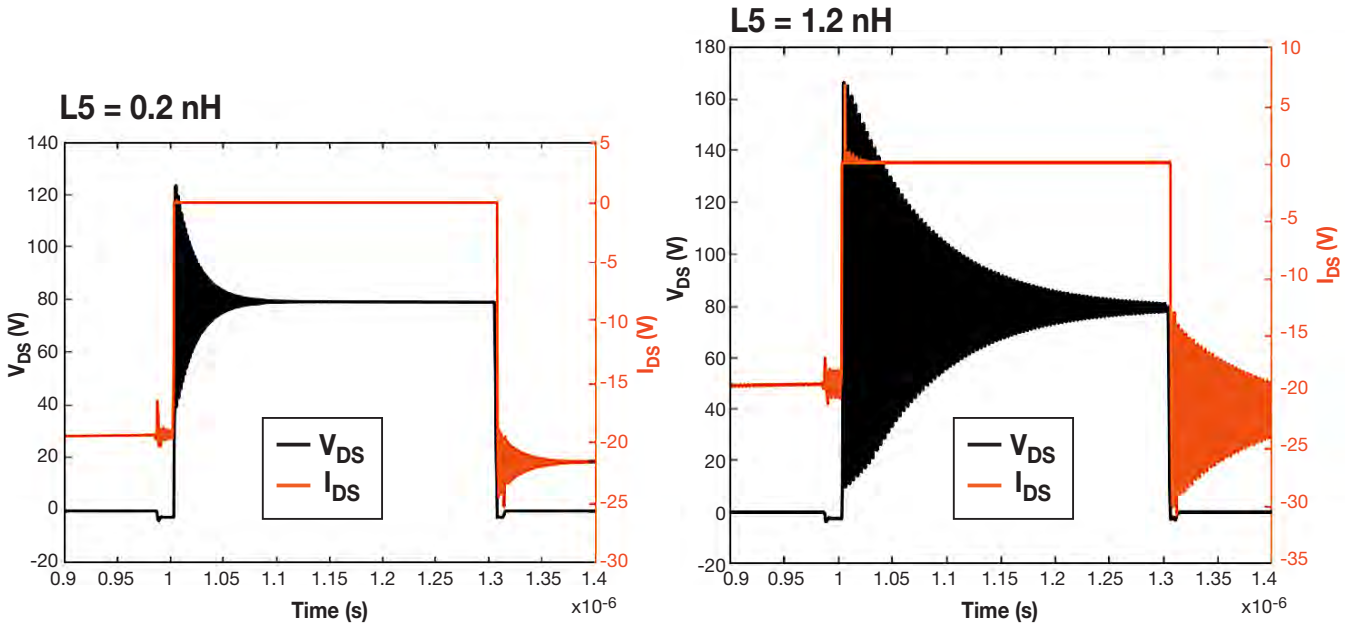


Figure 31: 48 V –12 V buck converter operating at 500 kHz. To produce different amounts of overshoot, L5 was varied from 0.2 nH to 1.2 nH. 0.2 nH resulted in a peak overshoot on the low-side device of 50 V above the 80 V DC bus (left), whereas a 1.2 nH inductor created a 90 V peak overshoot.

Figure 32 shows the amount of charge trapped in the first cycle as compared with the cumulative amount trapped in the 10 millionth cycle (Note the five orders of magnitude change in vertical axis and the high resolution of the scale). The red oval shows that, at some point from 1 to 10 million cycles, the characteristics changed. In fact, this is caused by the barrier height increasing slightly every time an electron is trapped. This makes it more difficult for all but the most energetic electrons to get trapped. This region includes some ringing, but the trapped electrons are due to the very small leakage current combined with the high V_{DS} when the device is nominally in the off state.

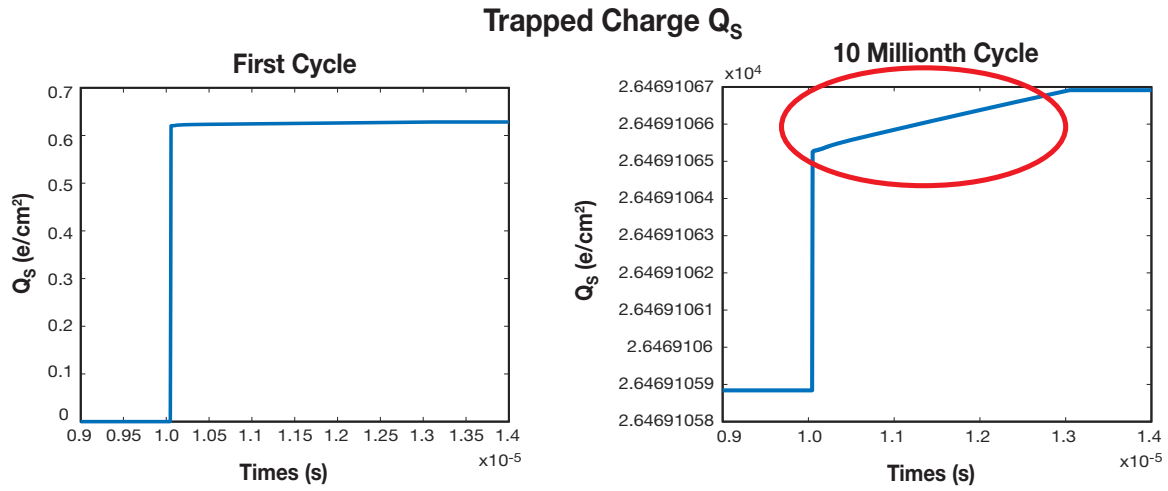


Figure 32: Amount of charge trapped Q_S in the first cycle as compared with the cumulative amount trapped in the 10 millionth cycle

These data can be translated into the graphs in Figure 33. The upper pair show the trapped charge, Q_S, over time on the left, and the normalized $R_{DS(on)}$ on the right for the 0.2 nH inductor case. The lower graphs show the same information for the 1.2 nH case. Whereas there is a minimal increase in $R_{DS(on)}$ with ringing as high as 130 V peak, there is more significant evolution of $R_{DS(on)}$ when peak voltages go as high as 170 V.

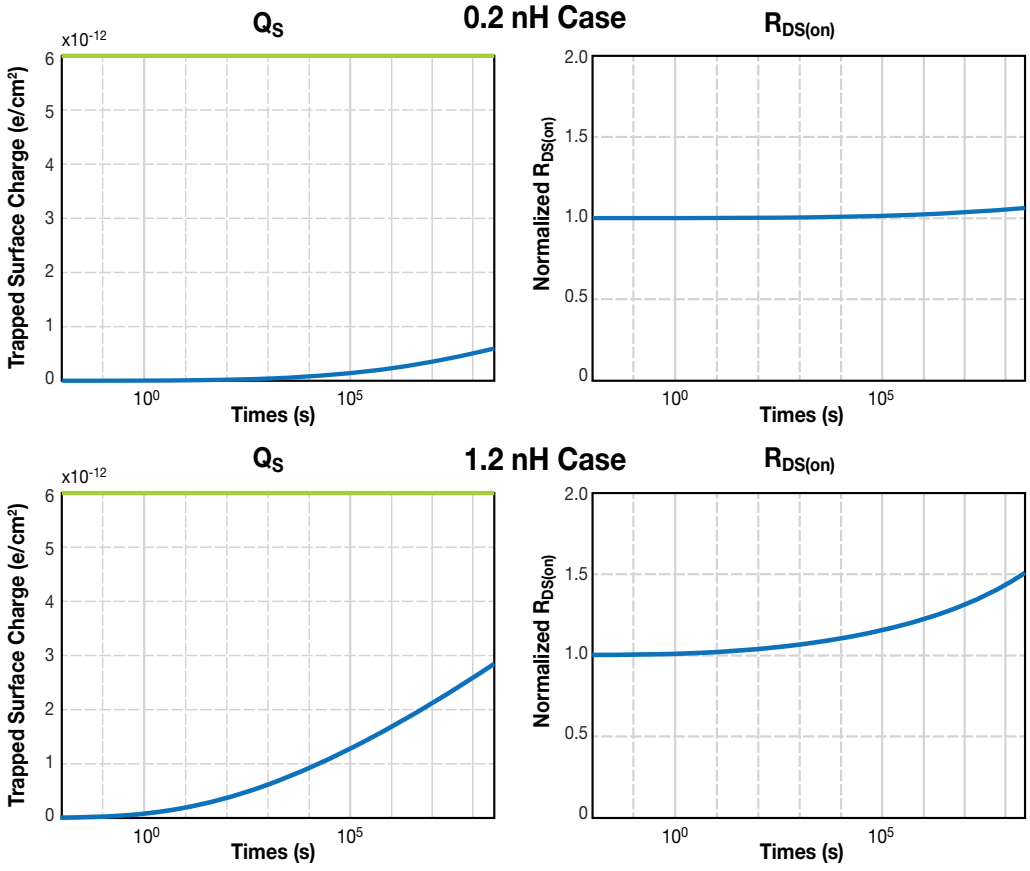


Figure 33: The upper pair of graphs show the trapped charge, Q_S, over time on the left, and the normalized, $R_{DS(on)}$, on the right for the 0.2 nH inductor case. The lower graphs show the same information for the 1.2 nH case.

3.6 High-Side GaN Transistor

In Figure 34 on the left are the current and voltage waveforms for the high-side control FET in the buck converter of Figure 30. This time the eGaN FET experiences hard-switching transitions at turn-on and turn-off. For the same value of L5 inductance (1.2 nH) the overshoot on the high-side device is only about 40 V, resulting in a peak overshoot voltage of 120 V. On the right are graphed the charge trapped in the first cycle (top) compared with the 10 millionth cycle (bottom). Noting the vertical scale change, as with the low-side transistor, the characteristics change as the amount of trapped charge increases in later cycles. There is a bump in charge that appears during the turn-off cycle at 1.3 µS that was not seen in the low-side device. In this part of the cycle the high-side transistor has a significant amount of current during the voltage decay in turn-off. There is therefore a significant supply of highly energetic electrons available for trapping.

As might be expected with the reduced peak overvoltage of 120 V on the high side device with 1.2 nH inductance, the minimal evolution of $dR_{DS(on)}$ is similar to that in Figure 33 for the 0.2 nH case as they both have about the same peak overshoot voltage as shown in Figure 35.

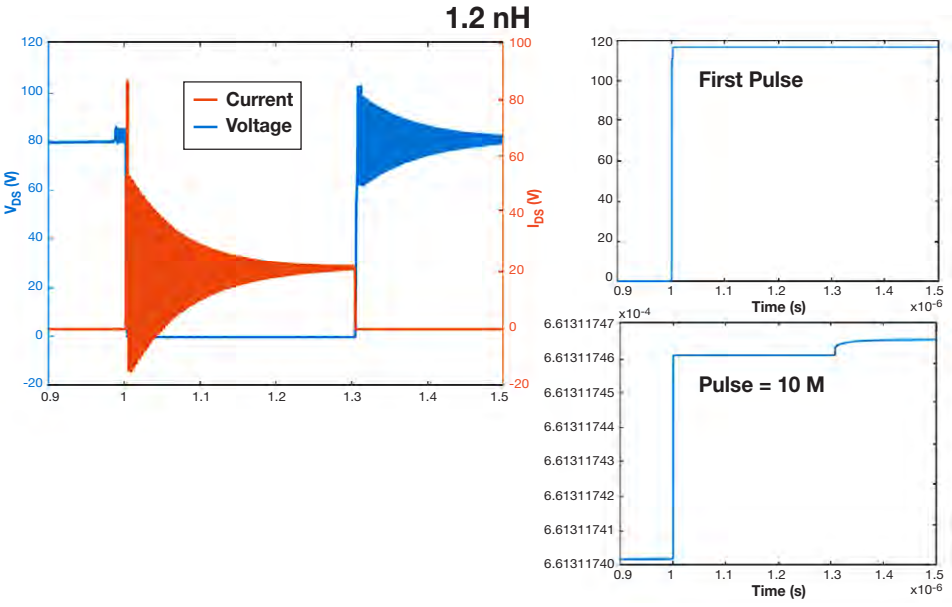


Figure 34: (left) Current and voltage waveforms for the high-side control FET in the buck converter of Figure 30. (right) Charge trapped in the first cycle (top) compared with the 10 millionth cycle (bottom).

3.7 Summary of Applying the Model to Important Real-World Use Cases

A physics-based model enables calculation of charge trapping for any given switching loci. Simulations show that current has a small impact, and voltage a much larger impact. In an LLC synchronous rectifier with a 12 V output, varying the leakage inductance from 50 pH to 150 pH on each leg of the transformer produced a different amount of overshoot, but not a significant amount of $dR_{DS(on)}$, even when using 30 V rated devices. In a buck converter, for both low side and high side transistors there was minimal change in $R_{DS(on)}$ up to 130 V peak overshoot for the 100 V rated device. At 170 V peak overvoltage, $R_{DS(on)}$ of this 100 V device degraded only 50% over 10 years.

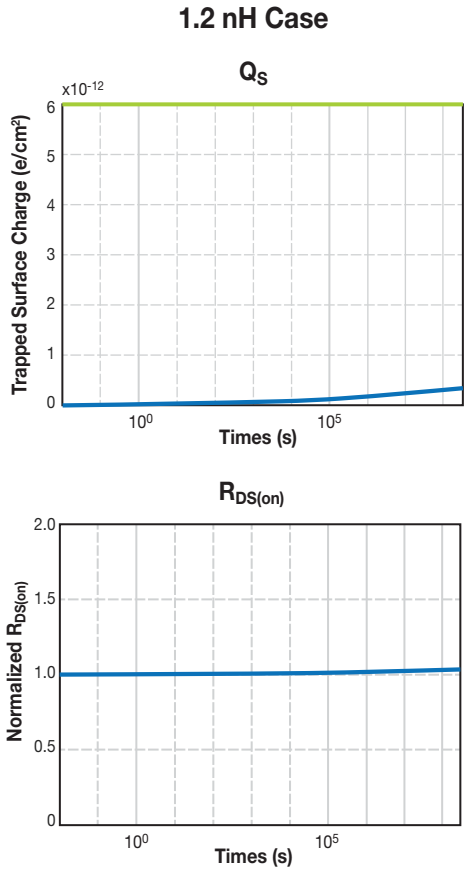


Figure 35: (Top) Trapped charge Q_S over time, and (bottom) normalized $R_{DS(on)}$. The horizontal scale ends on the right at 10 years.

SECTION 4: SAFE OPERATING AREA

Safe operating area (SOA) testing exposes the GaN transistor to simultaneous high current (I_D) and high voltage (V_{DS}) for a specified pulse duration. The primary purpose is to verify the transistor can be operated without failure at every point (I_D, V_{DS}) within the datasheet SOA graph. It is also used to probe the safety margins by testing to fail outside the safe zone.

During SOA tests, the high-power dissipation within the die leads to a rapid rise in junction temperature and the formation of strong thermal gradients. For sufficiently high power or pulse duration, the device simply overheats and fails catastrophically. This is known as thermal overload failure.

In Si MOSFETs, another failure mechanism known as secondary breakdown (or Spirito effect [2]) has been observed in SOA testing. This failure mode, which occurs at high V_D and low I_D, is caused by an unstable feedback between junction temperature and threshold V_{TH}. As the junction temperature rises during a pulse, V_{TH} drops, which can cause pulse current to rise. The rising current, in turn, causes temperature to rise faster, thereby completing a positive feedback loop that leads to thermal runaway and ultimate failure. A goal of this study is to determine if the Spirito effect exists in GaN transistors.

For DC, or long-duration pulses, the SOA capability of the transistor is highly dependent on the heatsinking of the device. This can present a huge technical challenge to assess the true SOA capability, often requiring specialty water-cooled heatsinks. However, for short pulses (< 1 ms), the heatsinking does not impact SOA performance. This is because on short timescales, the heat generated in the junction does not have sufficient time to diffuse to any external heatsink. Instead, all the electrical power is converted to raising the temperature (thermal capacitance) of the GaN film and nearby silicon substrate. As a result of these considerations, SOA tests were conducted at two pulse durations: 1 ms and 100 µs.

Figure 36 shows the SOA data of 200 V EPC2034C. In this plot, individual pulse tests are represented by points in (I_D, V_{DS}) space. These points are overlaid on the datasheet SOA graph. Data for both 100 µs and 1 ms pulses data are shown together. Green dots correspond to 100 µs pulses in which a part passed, whereas red dots indicate where a part failed. A broad area of the SOA was interrogated without any failures (all green dots), ranging from low V_{DS} all the way to V_{DSmax} (200 V). All failures (red dots) occurred outside the SOA, indicated by the green line in the datasheet graph. The same applies to 1 ms pulse data (purple and red triangles); all failures occurred outside of the datasheet SOA.

Figure 37 provides SOA data for three more parts, AEC EPC2212 (4th generation automotive 100 V), EPC2045 (5th generation 100 V), and EPC2014C (4th generation 40 V). In all cases, the datasheet safe operating area has been interrogated without failures, and all failures occur outside of SOA limits, often well outside the limits.

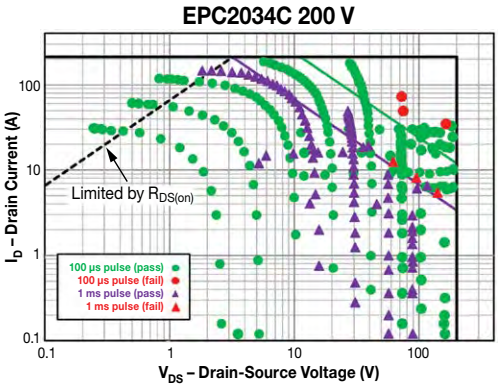


Figure 36: EPC2034C SOA plot. The "Limited by $R_{DS(on)}$" line is based on datasheet maximum specification for $R_{DS(on)}$ at 150°C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles (1 ms) or red dot (100 µs). Note that all failures occur outside the datasheet SOA region

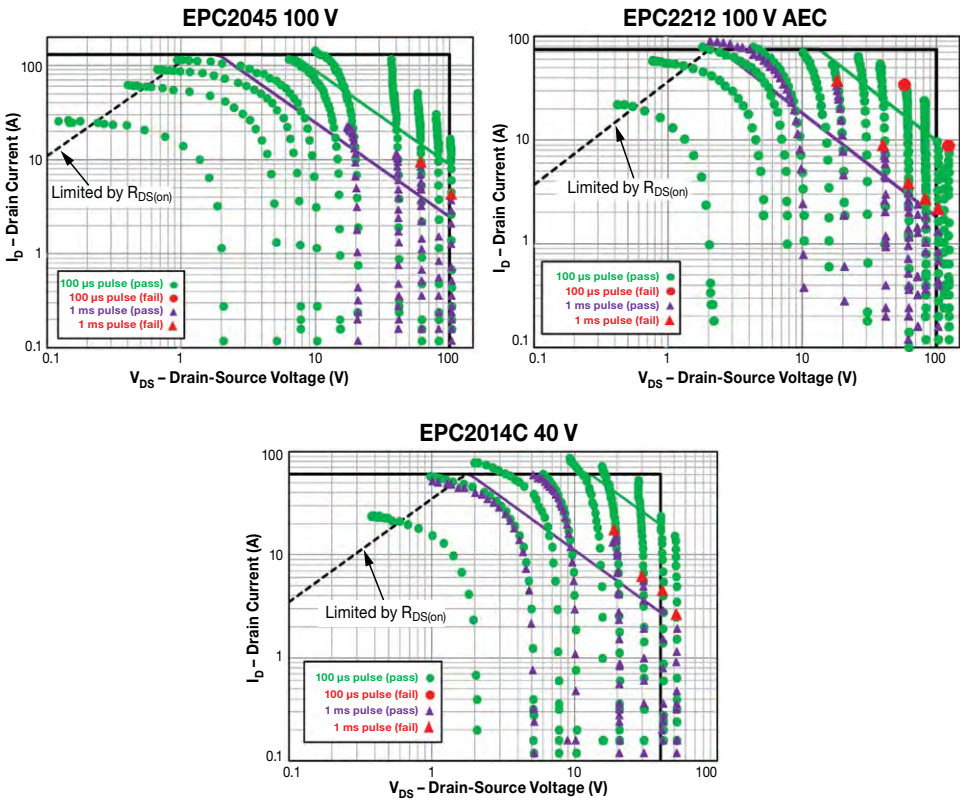


Figure 37: EPC2034C SOA plot. The "Limited by $R_{DS(on)}$" line is based on datasheet maximum specification for $R_{DS(on)}$ at 150°C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles (1 ms) or red dot (100 µs). Note that all failures occur outside the datasheet SOA region

The datasheet SOA graph template is generated with finite element analysis, using a thermal model of the device including all relevant layers along with their heat conductivity and heat capacity. Based on transient simulations, the SOA limits are determined by a simple criterion: for a given pulse duration, the power dissipation must be such that the junction temperature does not exceed 150°C before the end of the pulse. This criterion results in limits based on constant power, denoted by the 45° green (100 µs) and purple (1 ms) lines in the SOA graph. This approach leads to a datasheet graph that defines a conservative safe operating zone, as evidenced by the extensive test data in this study. In power MOSFETs, the same constant power approach leads to an overestimate of capability in the high voltage regime, where failure occurs prematurely due to thermal instability (Spirito effect).

While the exact physics of failure is yet to be determined, the main outcome of this study is clear – *GaN transistors will not fail when operated within their datasheet SOA*.

SECTION 5: SHORT-CIRCUIT ROBUSTNESS TESTING

Short circuit robustness refers to the ability of a FET to withstand unintentional fault conditions that may occur in a power converter while in the ON (conducting) state. In such an event, the device will experience the full bus voltage combined with a current that is limited only by the inherent saturation current of the transistor and the circuit parasitic resistance, which varies with the application and location of the fault. If the short-circuit state is not quenched by protection circuitry, the extreme power dissipation will ultimately lead to thermal failure of the transistor. The goal of short-circuit testing is to quantify the "withstand time" the part can survive under these conditions.

Typical protection circuits (e.g., de-saturation protection for IGBT gate drivers) can detect and react to over-current conditions in 2–3 µs. It is therefore desirable if the GaN transistor can withstand unclamped short-circuit conditions for about 5 µs or longer.

The two main test circuits used for short-circuit robustness evaluation are described in [35]:

- Hard-switched fault (HSF): gate is switched ON (and OFF) with drain voltage applied
- Fault under load (FUL): drain voltage is switched ON while gate is ON

For this study, devices were tested in both fault modes and no significant differences in the withstand time were found. Therefore, the focus will be on FUL results for the remainder of this discussion. However, it is important to note that from HSF testing, GaN transistors did not exhibit any latching or loss of gate control that can occur in silicon-based IGBTs [35]. This result was expected given the lack of parasitic bipolar structures with the GaN devices. Until the time the transistors fail catastrophically, the short circuit can be fully quenched by switching the gate LOW, an advantageous feature for protection circuitry design.

Two representative GaN transistors were tested:

1) EPC2203 (80 V): 4th generation automotive grade (AEC) device

2) EPC2051 (100 V): 5th generation device

These devices were chosen because they are the smallest in their product families. This simplified the testing owing to the high currents required for short-circuit evaluation. However, based on simple thermal scaling arguments, the withstand time is expected to be identical for other in-family devices. EPC2203 results cover EPC2202, EPC2206, EPC2201 and EPC2212; EPC2051 covers EPC2045 and EPC2053.

Figure 38 shows fault-under-load data on EPC2203 for a series of increasing drain voltages. With V_{GS} at 6 V (the datasheet maximum), and a 10 µs drain pulse, the device did not fail all the way up to V_{DS} of 60 V. Under these conditions, over 1.5 kW is dissipated in a 0.9 mm x 0.9 mm die. At the higher V_{DS}, the current is seen to decay over time during the pulse. This is a result of rising junction temperature within the device and does not signify any permanent degradation.

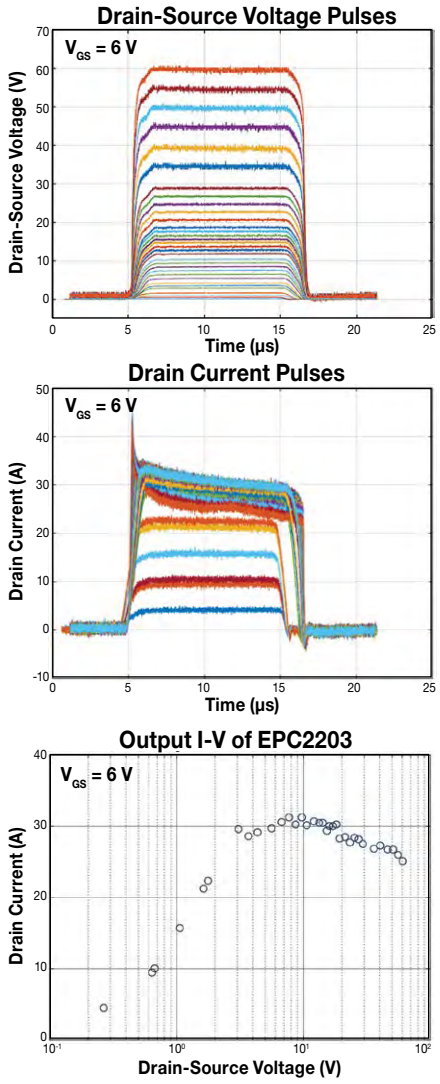


Figure 38: EPC2203 fault under load test (FUL) waveforms for a series of increasing drain voltages. Drain pulse is 10 µs and V_{GS} = 6 V. The device did not fail for this pulse width. V_{DS} vs. time. V_{DS} is Kelvin-sensed directly at the device terminals (left). I_{DS} vs. time. Note that I_{DS} decreases over time due to self-heating (center). Resulting output curve for this test sequence (right). Drain current is reported as the average current during the pulse. Drain current rolls over in the saturation region owing to device heating at higher V_{DS}.

Using a longer pulse duration (25 µs), the parts eventually fail from thermal overload. Representative waveforms are shown in Figure 39. The time of failure is marked by the abrupt sharp rise in drain current. After this event, the devices are permanently damaged. The withstand time is measured from the beginning of the pulse to the time of failure.

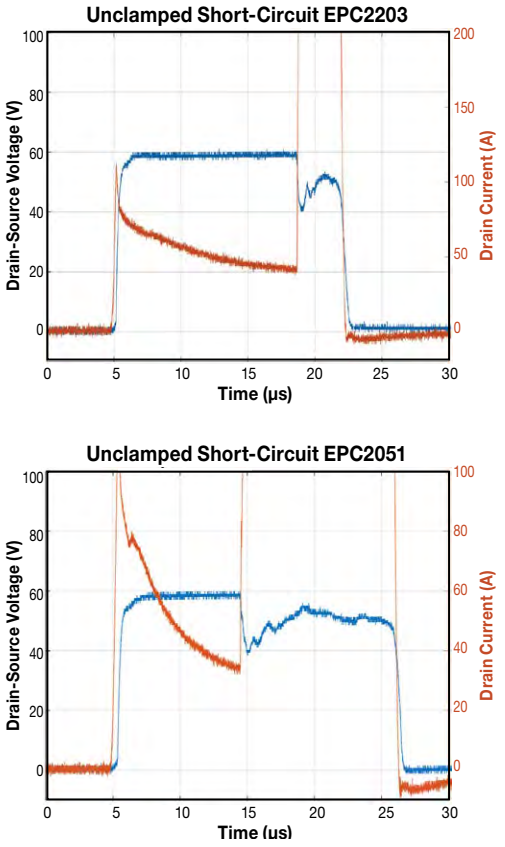


Figure 39: Fault-under-load test waveforms for a typical EPC2203 (top) and EPC2051 (bottom) at V_{DS} = 60 V, V_{GS} = 6 V, and a 25 µs drain pulse. The abrupt rise in drain current marks the time of catastrophic thermal failure.

To gather statistics on the withstand time, cohorts of eight parts were tested to failure using this approach. Table 3 summarizes the results. EPC2203 was tested at both 5 V (recommended gate drive) and 6 V ($V_{GS(max)}$), with mean withstand time of 20 µs and 13 µs respectively. Note that the device survives less time at 6 V because of the higher saturation current. EPC2051 exhibited a slightly lower time-to-fail (9.3 µs) compared with the EPC2203 at 6 V. This is expected because of the more aggressive scaling and current density of 5th generation products. However, in all cases, the withstand time is comfortably long enough for most short-circuit protection circuits to respond and prevent device failure. Furthermore, the withstand time showed small part-to-part variability.

The lower rows in Table 3 provide pulse power and energy relative to die size. To gain insight into the relationship between these quantities and the time to failure, time-dependent heat transfer was simulated to determine the rise in junction temperature ΔT_J during the short-circuit pulse. The results are shown in Figure 40.

Short-circuit pulse V_{DS} = 60 V	EPC2203 (Gen 4)		EPC2051 (Gen 5)	
	V_{GS} = 6 V	V_{GS} = 5 V	V_{GS} = 6 V	V_{GS} = 5 V
Mean TTF (µs)	13.1	20.0	9.33	21.87
Std. dev. (µs)	0.78	0.37	0.21	2.95
Min. TTF (µs)	12.1	19.6	9.08	18.53
Avg pulse power (kW)	1.764	1.4	3.03	2.03
Energy (mJ)	23.83	27.6	27.71	42.49
Die area (mm²)	0.9025		1.105	
Avg power/area (kW/mm²)	1.95	1.55	2.74	1.84
Energy/area (mJ/mm²)	26.4	30.59	25.08	38.46

Table 3: Short-circuit withstand time statistics for EPC2203 and EPC2051.

Note: Statistics derived from eight devices in each condition. Withstand times are tightly distributed around mean value. Average pulse power and energy correspond to a typical part within the population.

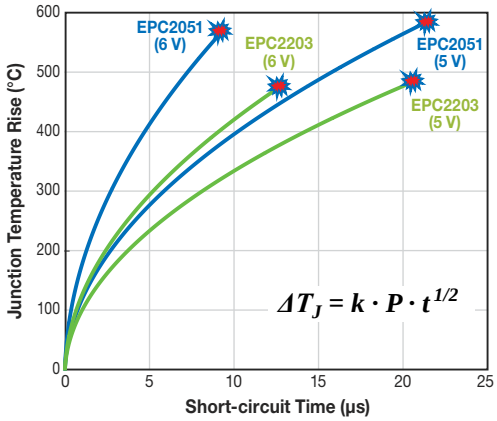


Figure 40: Simulated junction temperature rise versus time during the short-circuit pulses for both EPC2051 and EPC2203 at both 5 V and 6 V V_{GS}. Measured failure times are indicated by red markers. Note that EPC2203 fails catastrophically at a ΔT_J of around 475°C, whereas EPC2051 fails around 575°C. The simulated ΔT_J is well fit by a simple square root dependence on time (heat diffusion), as shown in the equation. *P* denotes the average power per unit area, and k = 6.73 x 10^{-5} K m²/W $s^{1/2}$.

The intense power density during the pulse leads to rapid heating in the GaN layer and nearby silicon substrate. Because the pulse is short and heat transfer is relatively slow, only a small thickness of semiconductor (< ~100 µm in depth) can help to absorb the energy. The temperature grows as the square root of time (characteristic of heat diffusion), and linearly with the pulse power. As can be seen in Figure 40, for EPC2203, both the 5 V and 6 V conditions fail at the same junction temperature rise of ~475°C. The same is true for EPC2051, where both conditions fail at the same ΔT_J of ~575°C. Three key conclusions stem from these results:

1) For a given device, the time to failure is inversely proportional to the power dissipation squared (P^{-2}). This applies for short-circuit and SOA pulses of duration < ~1 ms.
2) The intrinsic failure mode resulting from high power pulses is directly linked to the junction temperature exceeding a certain critical value.
3) Wide bandgap eGaN devices can survive junction temperatures (> 400°C) that are totally inaccessible to silicon devices owing to free-carrier thermal runaway.

To establish whether devices could survive these extreme conditions repetitively, several parts were subjected to over 500,000 cycles under short-circuit conditions that caused device currents about twice the maximum rated pulse current listed on their datasheets. In the test setup, gate bias of either 5 or 6 V_{DC} was applied to the gate of the device under test (DUT). Drain bias was set at 10 V_{DC} and a 60 mF capacitor was connected across the drain supply. A low $R_{DS(on)}$ high-side transistor in series with the DUT controlled the otherwise unlimited flow of current. The control transistor was then pulsed with 5-µs pulses at 1 Hz to give the channel time to re-equilibrate. Table 4 shows the various types of devices tested, their datasheet rating for maximum pulsed current, and the amount of short-circuit current that pulsed through the device during each cycle at the start of the test.

Device	Type	Datasheet pulsed (A)	V_{GS}	Mean (A)	Sigma (A)
EPC2203	80 V AEC Gen4	17	5	35	2.4
			6	43	2.5
EPC2212	100 V AEC Gen4	75	5	124	2.1
			6	160	3.5
EPC2051	100 V Gen5	37	5	68	1.0
			6	87	1.3
EPC2052	100 V Gen5	74	5	147	1.6
			6	163	2.2
EPC2207	200 V Gen5	54	5	99	4.7
			6	132	5.0

Table 4: Devices tested under extreme pulsed short circuit current, typically twice the maximum datasheet limit

Table 5 shows the various key device parameters for the EPC2051, the same part number as used in Table 3 and in Figure 40. Even under these extreme conditions of 500,000 85 A pulses that are more than twice the datasheet maximum ratings, all electrical characteristics remained within datasheet specifications. There was, however, a small reduction in the amount of short circuit current "consumed" by the DUT over time, consistent with the small increase in V_{TH}.

After this 500 k pulse sequence, this part underwent an unbiased 10 minute anneal at 175°C. As can be seen in the right-hand column of Table 5, the electrical parameters and short-circuit current recovered to near their values before being subjected to repetitive pulse stresses. This recovery indicates that no permanent damage occurred from repetitive high-current pulses.

EPC2051	t = 0	100 k pulses	500 k pulses	Post 10 min. 175°C Anneal
V_{TH} (V)	1.8	2	2.1	1.8
I_{GSS} (µA)	11	33	55	23
I_{DSS} (µA)	7	5.5	5.1	5.6
$R_{DS(on)}$ (mΩ)	22	22.3	22.3	22
$I_{short\ circuit}$	84	77	74	82

Table 5: Key device parameters for EPC2051 at the start of pulse testing, after 100 k pulses, after 500 k pulses, and after a 175°C, 10 minute anneal. Device parameters stayed within datasheet limits at all times.

SECTION 6: HIGH di/dt CURRENT PULSE RELIABILITY (Lidar Application)

GaN transistors and ICs are widely implemented in both direct time-of-flight (DToF) and indirect time-of-flight (IToF) light detection and ranging (lidar) circuits for autonomous vehicles. Chapter 5 of EPCs latest text book, ***GaN Power Devices and Applications*** goes into detail on this topic.

In a typical DToF lidar application, the GaN device delivers short, high current pulses, on the order of 1–5 ns, which drive a laser diode to generate narrow optical pulses [36]. The peak currents are usually substantially greater than 50% of the transistor pulse-current rating. The pulse duty cycle is typically low, and the pulse repetition frequency is in the range of 10 to 100 kHz. When not being pulsed, the GaN device is in the OFF state, exposed to a certain drain bias.

This stress condition is unprecedented for a power device, making it difficult to predict lifetime in operation by relying on conventional DC reliability tests such as high temperature gate bias (HTGB) or high temperature reverse bias (HTRB). The simultaneous high current and voltage during a pulse raises concerns about hot-carrier effects, potentially leading to threshold voltage (V_{TH}) or on-resistance ($R_{DS(on)}$) shifting within the device. In addition, the cumulative effect of repetitive high current pulses raises the specter of electro-migration leading to degradation of the solder joints.

Even GaN-specific tests, like the hard-switching reliability testing originally discussed in [37], do not effectively emulate the stress conditions in a lidar circuit. To address these concerns a novel test method was developed in collaboration with several lidar sensor manufacturers. This lidar reliability testing is part of a "Beyond AEC" initiative described in [38], which is a series of GaN specific stress tests that go beyond the conventional reliability tests developed for MOSFETs as part of AEC-Q101 standard.

6.1 Long-term Stability under HIgh Current Pulses

The concept of this test method is to stress parts in an actual lidar circuit for a total number of pulses well beyond their ultimate mission profile. The mission profiles for automotive lidar vary from customer to customer. A typical automotive profile would call for a 15-year life, with two hours operation per day, at 100 kHz pulse repetition frequency (PRF). This corresponds to approximately four trillion total lidar pulses. Some worst-case (heavy use) scenarios might call for as many as 10–12 trillion pulses in service life.

By testing a population of devices well beyond the end of their full mission profile while verifying the stability of the system performance and the device characteristics, this test method directly demonstrates the lifetime of eGaN devices in a lidar mission.

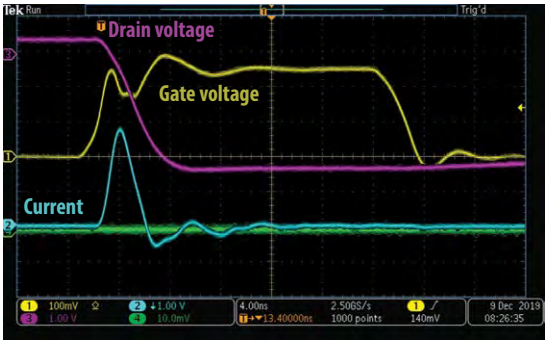
6.2 Test Methodology and Results

To achieve the large number of pulses, parts are stressed continuously at a pulse repetition frequency (PRF) much higher than in typical lidar circuits.

For this study, two popular AEC grade parts were put under test: EPC2202 (80 V) and EPC2212 (100 V). Four parts of each type were tested simultaneously. During the stress, two key parameters were continuously monitored on every device: (1) peak pulse current and (2) pulse width. These parameters are both critical to the range and resolution of a lidar system.

Figures 41 and 42 show the results of this test over the first 13 trillion pulses.

The cumulative number of pulses well exceeds a typical automotive lifetime and covers worst-case use conditions. Note that there is no observed degradation or drift in either the pulse width or height. While this is an indirect monitor of the health of the GaN device, it indicates that no degradation mechanisms have occurred that would adversely impact lidar performance.



AEC-Q101 series of discrete FETs

- 8 samples (>7000h)
- 0 failures and perfect pulse stability

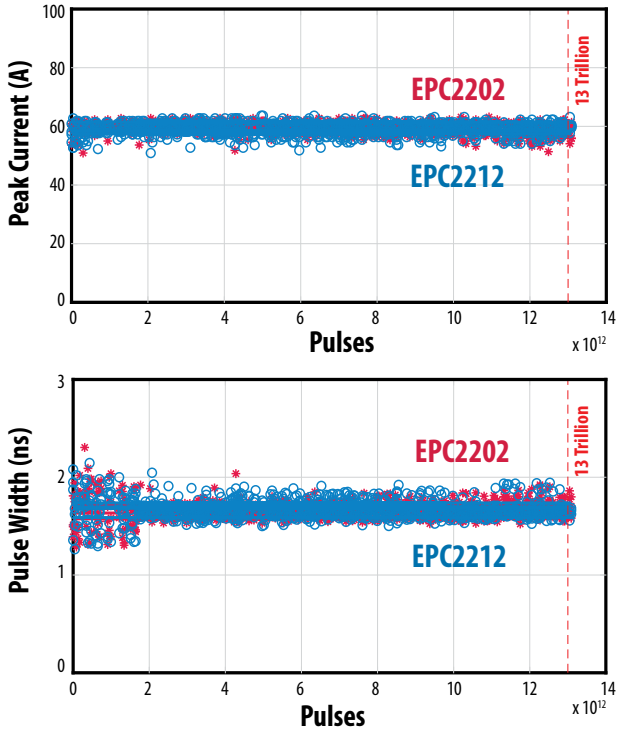


Figure 41: Long-term stability of pulse width (bottom right) and pulse height (top right) over 13 trillion lidar pulses. Data for four EPC2202 (red) devices and four EPC2212 (blue) devices are overlaid in the plots. Note the excellent stability of these key parameters over a total number of pulses corresponding to an automotive lifetime in heavy-use conditions.

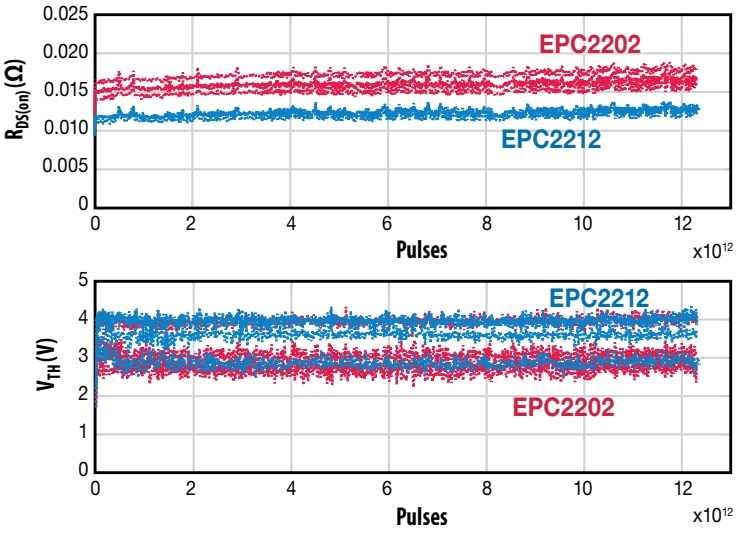


Figure 42: Long-term stability of $R_{DS(on)}$ and V_{TH} during lidar reliability testing. These parameters are measured at six-hour intervals on every part by briefly interrupting the lidar stress. Note that V_{TH} is inferred by measuring $R_{DS(on)}$ at a series of gate voltages. Data for four EPC2202 (red) devices and four EPC2212 (blue) devices are overlaid in the plots. Note the excellent stability of these key parameters over 13 trillion pulses, corresponding to an automotive lifetime under heavy-use conditions.

SECTION 7: MECHANICAL STRESS

The ultimate lifetime of a product, or its suitability in a given application, may be limited by the mechanical stresses encountered. In this section, some of the most common mechanical stressors, die shear, backside pressure, and bending force are characterized, and the WLSCP package is demonstrated to be robust under normal assembly or mounting conditions.

7.1 Die Shear Test

The purpose of die shear test is to evaluate the integrity of the solder joints used to attach eGaN devices to PCBs. This determination is based on the in-plane force at which, when applied to a mounted device, the die shears off from the PCB. All testing followed the military test standard, MIL-STD-883E, Method 2019 [39].

Figure 43 shows the test results of four selected GaN transistors. Ten parts were tested for each product. The smallest die tested is EPC2036/EPC2203, which only has four solder balls with a diameter of 200 µm and a die area of 0.81 mm^2. As expected, this product turned out to have the least shear strength, however, it exceeds the minimum force requirement specified by the MIL standard, as shown in Figure 43. The largest die tested was EPC2206, a land grid array (LGA) product with die area of 13.94 mm^2. EPC2206 exceeds the minimum force requirement more than a factor of ten. Within the size spectrum, two additional products were tested: EPC2212 (100 V LGA) and EPC2034C (200 V BGA). Both products surpassed the minimum force significantly.

In Figure 43, the results show that all WLCSP GaN products are mechanically robust against environmental shear stress under the most stringent conditions.

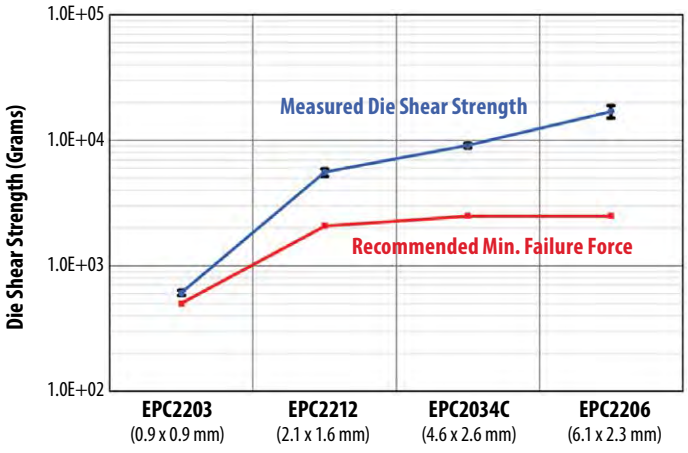


Figure 43: Various die sizes and solder configurations of GaN transistors were tested to failure while measuring the shear strength. The results are shown with black dots. The red dots show the minimum recommended die shear strength under MIL-STD-883E, Method 2019.

7.2 Backside Pressure Test

Another critical aspect of the mechanical robustness of GaN devices is how well they handle backside pressure. This is an important consideration for applications that require backside heatsinking to the die. It is also important to determine the safe "pick-and-place" place force during assembly.

Backside pressure tests up to 400 psi were performed, where the pressure is calculated by the force applied divided by the die area. Figure 44 shows the laboratory pressure tester that was employed. The pressure was applied directly to the backside of the die using a loading speed of 0.6 mm/min. Before and after the pressure test, parametric testing was performed to determine pass or fail. Subsequently, the parts were exposed to humidity-bias testing (H3TRB) at 60 V_{DS}, 85°C, and 85% relative humidity for 300 hours. H3TRB is effective to determine if there were any latent failures caused by mechanical damage (internal cracking) from the pressure test.

Figure 44: Pressure test instrument. The tester head lowers to the backside of the devices using a constant loading speed of 0.6 mm/min until the predetermined force is sensed by the gauge. The DUTs are surface mounted on a FR4 test coupon that is secured on the testing stage.

EPC2212 (100 V, LGA) and EPC2034C (200 V, BGA) were tested and both passed 400 psi. The data is included in Table 6. These results show that eGaN FETs have enough margin to handle backside pressure that is normally used at a PCB assembly house. Though these parts survived 400 psi, EPC recommends limiting maximum backside pressure to 50 psi or less.

Product	Sample Size	Die Area	Backside Pressure	Force Applied	Failures in Parametric Test after Pessure Test	Failures after 300 hours H3TRB test
EPC2212 (LGA)	16	2.1 x 1.6 mm	400 psi	9.3 N (2.1 lbs)	0/16	0/16
EPC2034C (BGA)	16	4.6 x 2.6 mm	400 psi	33.0 N (7.4 lbs)	0/16	0/16

Table 6: eGaN device pressure results.

Note: Small and relatively large eGaN devices were tested under high backside pressure with no mechanical failures, and no failures after stress testing under temperature, humidity, and bias.

7.3 Bending Force Test

The purpose of the bending force test is to determine the ability of a GaN transistor to withstand flexure of the PCB which might occur during handling, assembly, or operation. Though this test standard was developed for passive surface mount components (AEC-Q200) [40], many customers have concerns about bending forces on GaN transistors for two main reasons: (1) robustness of the WLCSP solder joints; and (2) piezoelectric effects within the transistor that may alter device parametrics and disrupt circuit operation.

To address these concerns, bending force testing on four EPC2206 devices following the AEC-Q200-005A test standard [41] were conducted. Figure 45 shows a schematic of the test setup. Devices are assembled near the center of an FR4 PCB (100 mm long x 40 mm wide x 1.6 mm thick). With ends rigidly clamped, a force is applied on the opposite side from the device, leading to an upward deflection of the PCB. After a 60 second dwell in this flexed state, all device electrical parameters are measured.

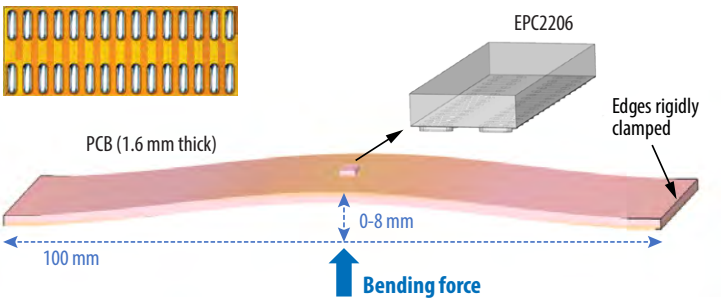


Figure 45: Schematic depiction of bending force (AEC-Q200-005A) test for EPC2206. Force is applied on the bottom of the board. Force is adjusted to attain a set of prescribed center point deflections ranging from 0–8 mm.

To address these concerns, bending force testing on four EPC2206 devices following the AEC-Q200-005A test standard [39] were conducted. Figure 45 shows a schematic of the test setup. Devices are assembled near the center of an FR4 PCB (100 mm long x 40 mm wide x 1.6 mm thick). With ends rigidly clamped, a force is applied on the opposite side from the device, leading to an upward deflection of the PCB. After a 60 second dwell in this flexed state, all device electrical parameters are measured.

The Q200-005A test standard calls for the force to be applied only once, with a 2 mm deflection of the PCB. However, consistent with test-to-fail philosophy, devices were tested at four progressively increasing deflections: 2 mm, 4 mm, 6 mm, 8 mm. An extreme force of 240 N (25 kg) is required to achieve 4 mm deflection. At each force level, all device parameters were measured (while flexed) following a 60 second soak period.

Table 7 shows normalized $R_{DS(on)}$ versus board deflection for all four devices under test. All devices passed the 2 mm test requirement. Two devices failed at 6 mm deflection, while the remaining two survived all the way to 8 mm. Postmortem analysis revealed that the failure mode was solder joint cracking, leading to an open gate connection. Up until failure, $R_{DS(on)}$ did not show any appreciable response to board flexure. The same was observed in other electrical characteristics like V_{TH} and I_{DSS}.

	0 mm	2 mm	4 mm	6 mm	8 mm
DUT1	1.00	1.01	1.00	0.98	0.98
DUT2	1.00	1.02	1.01	*Failed*	-
DUT3	1.00	1.01	1.03	*Failed*	-
DUT4	1.00	0.99	0.99	1.03	1.04

Table 7: Normalized $R_{DS(on)}$ versus board deflection for four devices during bending force test. Values are normalized to the $R_{DS(on)}$ in the unflexed case. Two of four devices failed at 6-mm deflection, while the remaining two devices survived 8 mm. No significant stress response was seen in any device parameter.

To gain further insight into the failure mode and electrical response under bending forces, a finite element (FEA) simulation was made using a full mechanical model of the EPC2206 mounted on the PCB. These simulations calculate the mechanical deflection, stress/strain, and piezoelectric response inside the device.

Figure 46 shows the longitudinal stress in the EPC2206 solder joints for a bending force corresponding to a 6 mm deflection. (Stress is measured along the axis perpendicular to the PCB). As can be seen, the outer edges of the solder bars experience high tensile stress, while the inner edges are under compression. The peak tensile stress reaches ~6 x 10^8 N/m^2, which is beyond the quoted tensile yield stress limit for SAC305 solder (~3 x 10^8 N/m^2). This explains the observed solder joint cracks in the two parts failing at 6-mm deflection.

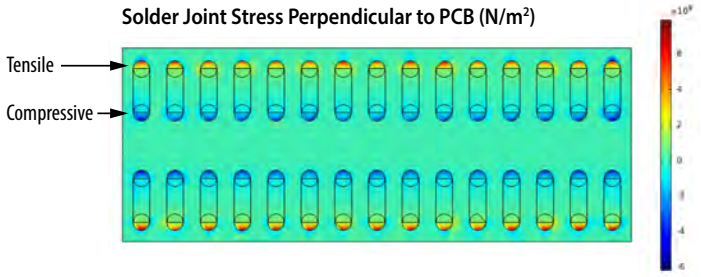


Figure 46: FEM simulations of the longitudinal stress in EPC2206 solder joints along the direction perpendicular to the plane of PCB (6 mm deflection bending force). Outer edges of the solder bars experience high tensile stress near yield stress limit for the solder joint.

Piezoelectric and spontaneous polarization in AlGaN/GaN HEMTs has a first order impact on device operation. In fact, the polarization sheet charge (~1.0 x 10^{13} e$^-$/cm^2) at the AlGaN/GaN interface is directly responsible for the high electron density in the 2DEG channel of GaN transistors. This charge has a direct (linear) impact on V_{TH} and $R_{DS(on)}$ As a result, concerns have been raised about the impact of piezoelectrically induced changes in device parameters when the part is under mechanical stress, such as in the bending test.

To address this concern, FEA was used to calculate the change in polarization sheet charge at the AlGaN/GaN heterojunction because of the extreme strain induced by the board bending experiments. The change in sheet charge is calculated via:

$$\Delta P_z = e_{zz}\epsilon_z + e_{zx}\left(\epsilon_x + \epsilon_y\right)$$
$$e_{zz} = 0.183\ C/m^2$$
$$e_{zx} = e_{zy} = -0.0275\ C/m^2 \qquad \text{Eq. 28}$$

where ε_z refers to strain along the (wurtzite) c-axis, and ε_x and ε_y refer to strain in the plane of the 2DEG. The effective piezoelectric constants e_{zz} and e_{zx} are derived from considering the difference in piezoelectric coefficients between GaN and AlGaN, as provided from *ab initio* calculations in Bernardini et al. [42].

Figure 47 shows the fractional change in polarization sheet charge inside the EPC2206 because of an extreme (4 mm) board deflection. At this level of mechanical stress, the solder joints are just below the threshold of failure for cracking. Polarization is normalized to the built-in

(zero strain) sheet charge of 1.0 x 10^{13} e^-/cm^2. The area averaged change in piezoelectric charge is less than −0.3%, while the peak change is around 0.8% in the immediate vicinity of solder bars. These changes in piezoelectric polarization are too small to create observable changes in device parameters V_{TH} or $R_{DS(on)}$. This explains why these parameters were not observed to change in any of the bending stress states. While piezoelectricity plays an important role in the device physics of GaN transistors, it is practically impossible to create sufficient mechanical strain inside the transistor to cause significant changes in device operation. As a result, typical stresses caused by vibration or board flexure do not present any circuit issues to the transistor in operation.

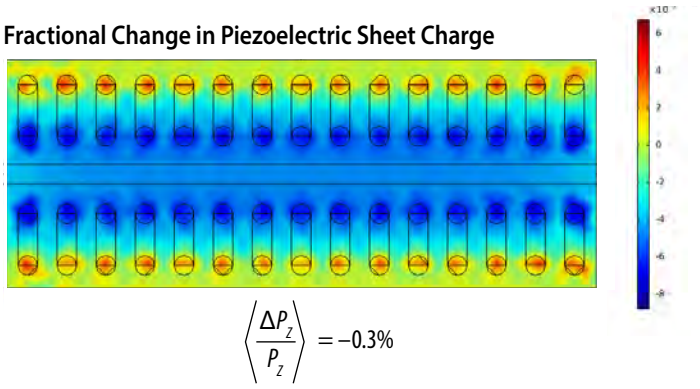


Figure 47: Fractional change in piezoelectric sheet charge for an EPC2206 under strain from 4 mm board deflection. The area averaged change in piezoelectric charge is less than −0.3%, while the peak change is around 0.8% in the immediate vicinity of solder bars. These changes in piezoelectric polarization are too small to create observable changes in device parameters V_{TH} or $R_{DS(on)}$.

SECTION 8: THERMO-MECHANICAL STRESS

GaN transistors in WLCSP have excellent thermo-mechanical reliability when tested according to AEC or JEDEC standards. This is because of the inherent simplicity of the "package," the lack of wire bonds, dissimilar materials, or mold compound. In summary, all WLCSP GaN transistors are capable of −40°C to 150°C in bare die form.

In addition to the component-level reliability, there are other industry specific standards like IPC-9592, or OEM environmental requirements that impose system or board-level tests for components mounted on a PCB. Among these, there is always a subset that induces severe thermo-mechanical stress on surface-mounted parts such as GaN transistors, and especially on the solder joints between the parts and the board. For instance, the most stringent temperature cycling requirement (Class II Category 2) from the IPC-9592 standard calls for 700 cycles at −40°C to 125°C without failure in a sample size of 30 units.

The reliability of the solder attachments depends on several factors that are independent of the device, including the PCB layout, design and material, the assembly process, the heatsinking solution in operation, and the nature of the application. Therefore, providing a precise model to predict time to failure in a particular application becomes infeasible and impractical. Nevertheless, in the past, EPC published a model to predict time to failure of solder joints based on the correlation between strain energy density and fatigue lifetime [43].

More Temperature Cycling, and Intermittent Operating Life (also known as Power Temperature Cycling) results are presented under different conditions. In addition, this section provides data and analysis on how to improve solder joint reliability with the use of underfill materials. Underfills are commonly used in applications that may expose surface-mount devices to the harshest environmental conditions.

It is important to emphasize that underfill is not required to ensure proper operation of WLCSP GaN transistors. In fact, for most of the reliability tests conducted during product qualification, the devices under test are mounted on FR4 boards with no underfill. The list of tests includes HTRB, HTGB, H3TRB, uHAST, MSL1, IOL, HTOL, ELFR, HTS and in many cases TC. However, underfill may be used for improved board-level reliability, since it reduces the stress on the solder joints resulting from coefficient of thermal expansion (CTE) mismatches between the die and PCB. Moreover, underfill provides pollution protection and additional electrical isolation in those cases with strict creepage and clearance requirements. Finally, underfill also helps in reducing the junction-to-board thermal impedance since the materials used have higher thermal conductivity than air, although lower than typical thermal interface materials. Note that the incorrect choice of an underfill material could also worsen solder joint reliability. Therefore, this section provides guidelines based on simulation and experimental results.

8.1 Criteria for Choosing a Suitable Underfill

The selection of underfill material should consider a few key properties of the material as well as the die and solder interconnections. Firstly, the glass transition temperature of the underfill material should be higher than the maximum operating temperature in application. Also, the CTE of the underfill needs to be as close as possible to that of the solder since both will need to expand/contract at the same rate to avoid additional tensile/compressive stress in the solder joints. As a reference, typical lead-free SAC305 and Sn63/Pb37 have CTEs of approximately 23 ppm/°C. Note that when operating above the glass transition temperature (Tg), the CTE increases drastically. Besides Tg, and CTE, the Young Modulus is also important. A very stiff underfill can help reduce the shear stress in the solder bump, but it increases the stress at the corner of the device, as it will be shown later in this section. Low viscosity (to improve underfill flow under the die) and high thermal conductivity are also desirable properties. Table 8 compares the key material properties of the underfills tested in this study.

Manufacturer	Part number	CTE (ppm/C)			Storage modulus (DMA) at 25°C (N/mm^2)	Viscosity at 25°C	Poisson's ratio	Volume resistivity	Thermal conductivity	Dielectric strength
		Tg (TMA) [C]	Below Tg	Above Tg						
HENKELS LOCTITE	ECCOBOND-UF 1173	160	26	103	6000	7.5 Pa*S				
NAMICS	U8437-2	137	32	100	8500	40 Pa*S	0.33	>1E15 Ω-cm	0.67 W/m·K	
NAMCIS	XS8410-406	138	19	70	13000	30 Pa*S				
MASTERBOND	EP3UF	70	25-30	75-120	3400	10-40 Pa*S	0.3	>1E14 Ω-cm	1.4 W/m·K	450 V/mil
AI TECHNOLOGY	MC7885-UF	236	20		7500	10 Pa*S		>1E14 Ω-cm	1 W/m·K	750 V/mil
AI TECHNOLOGY	MC7885-UFS	175	25		7500	10 Pa*S		>1E14 Ω-cm	2 W/m·K	1000 V/mil

Table 8: Underfill material properties

8.2 Underfill Study under Temperature Cycling

This section provides Temperature Cycling (TC) results of various GaN transistors under two different conditions, with and without the underfill materials listed earlier. Two temperature cycle ranges were tested: (i) –40°C to 125°C; and (ii) –55°C to 150°C. For all cases, the parts were mounted on DUT cards or coupons consisting of a 2-layer, 1.6 mm thick, FR4 board. SAC305 solder paste and water-soluble flux was used, followed by a flux clean process prior to the underfill. Temperature Cycling data for EPC2701C and EPC2053 are provided in Tables 9 –12 and results for EPC2206 are provided in the Weibull plot in Figure 48.

For both temperature ranges, the Namics underfills (U8437-2_N and 8410-406B) provide a large lifetime advantage compared to no underfill. The same applies to the Henkels (UF1137_H). On the other hand, Masterbond EP3UF was found to degrade the reliability. This was primarily the result of the low Tg, which meant that the underfill was exercised well beyond its glass transition temperature in all our studies. However, based on material properties, it is suspected that Masterbond EP3UF may be a suitable candidate for applications staying below 70°C.

Product/DOE	EPC2001C										
Stress condition: -40°C to 125°C	Status	300 cycles	550 cycles	850 cycles	1000 cycles	1250 cycles	1550 cycles	1750 cycles	1950 cycles	2150 cycles	2450 cycles
No Underfill	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	2/32 fails	5/32 fails	8/32 fails	15/32 fails	20/32 fails	26/32 fails
	On-going	0/32 fail	0/32 fail	0/32 fail	0/32 fail						
Henkels UF1137_H	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					
Masterbond EP3UF_M	On-going	0/40 fail	0/40 fail	14/40 fails	31/40 fails						
MC7685-UFS	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	1/32 fails	2/32 fails	2/32 fails	3/32 fails	6/32 fails	14/32 fails
MC7885-UF	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	1/32 fails	4/32 fails
Namics 8410-406B	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
Namics U8437-2_N	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
	On-going	0/80 fail	0/80 fail	0/80 fail	0/80 fail	0/80 fail					

Table 9: –40°C to 125°C Temperature Cycling results for EPC2001C

Product/DOE	EPC2053										
Stress condition: -40°C to 125°C	Status	300 cycles	550 cycles	850 cycles	1000 cycles	1250 cycles	1550 cycles	1750 cycles	1950 cycles	2150 cycles	2450 cycles
No Underfill	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	2/32 fails	3/32 fails	3/32 fails	3/32 fails
Henkels UF1137_H	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					
Masterbond EP3UF_M	On-going	1/40 fails	7/40 fails	15/40 fails	25/40 fails	39/40 fails					
MC7685-UFS	Completed	0/32 fail	0/32 fail	0/32 fail	1/32 fails	17/32 fails	32/32 fails	32/32 fails			
MC7885-UF	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	1/32 fails	1/32 fails	1/32 fails
Namics 8410-406B	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
Namics U8437-2_N	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					

Table 10: –40°C to 125°C Temperature Cycling results for EPC2053.

Product/DOE	EPC2001C					
Stress condition: -55°C to 150°C	Status	300 cycles	600 cycles	900 cycles	1100 cycles	1300 cycles
No Underfill	Completed	0/16 fail	0/16 fail	1/16 fails	1/16 fails	2/16 fails
Henkels UF1137_H	On-going	0/20 fail	0/20 fail	0/20 fail	1/20 fails	
Masterbond EP3UF_M	On-going	0/20 fail	0/20 fail	4/20 fails	6/20 fails	
MC7685-UFS	Completed	0/16 fail	0/16 fail	0/16 fail	1/16 fails	1/16 fails
MC7885-UF	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
Namics 8410-406B	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
Namics U8437-2_N	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
	On-going	0/20 fail	0/20 fail	0/20 fail	0/20 fail	

Table 11: –55°C to 150°C Temperature Cycling results for EPC2001C

Product/DOE	EPC2053					
Stress condition: -55°C to 150°C	Status	300 cycles	600 cycles	900 cycles	1100 cycles	1300 cycles
No Underfill	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	1/16 fails
Henkels UF1137_H	On-going	0/20 fail	0/20 fail	0/20 fail	0/20 fail	
Masterbond EP3UF_M	On-going	5/20 fails	15/20 fails			
MC7685-UFS	Completed	1/16 fails	9/16 fails	13/16 fails		
MC7885-UF	Completed	2/16 fails	1/16 fails	7/16 fails		
Namics 8410-406B	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
Namics U8437-2_N	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail

Table 12: –55°C to 150°C Temperature Cycling results for EPC2053

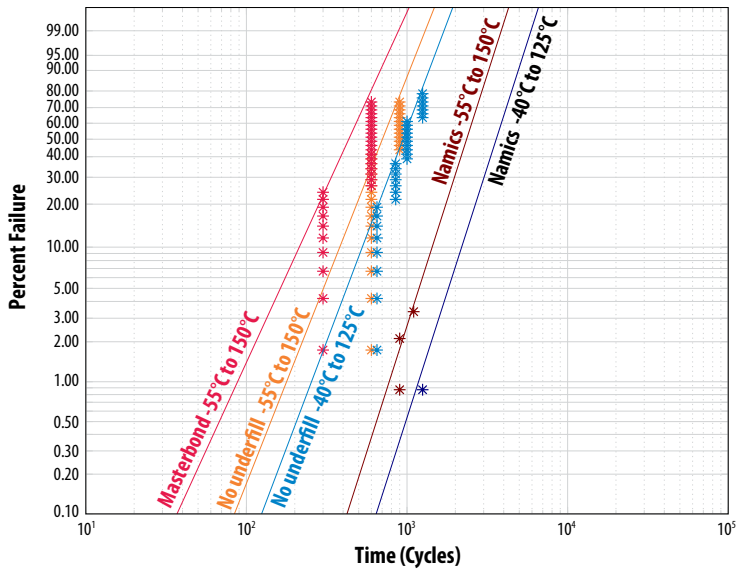
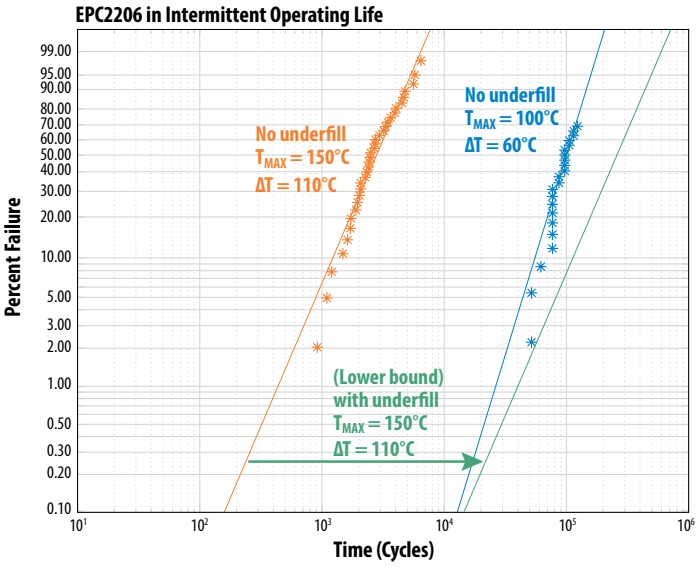


Figure 48: Weibull plots of Temperature Cycling results of EPC2206

8.3 Intermittent Operating Life Study

In Temperature Cycling, both the device and PCB are placed inside a chamber that cycles the ambient temperature, leading to an isothermal temperature change across the assembly. In Intermittent Operating Life (IOL), temperature rise is realized by dissipating power inside the device. Therefore, in IOL only the device and the PCB in the vicinity of the die change in temperature. As a result, the stresses on the solder joints resulting from the CTE mismatch between the GaN transistors and PCB are not as high as in Temperature Cycling. However, the time to complete a full cycle is much faster than in TC (Note that IOL may also be known as Power Temperature Cycling).

Figure 49 shows the results of a group of 32 samples of EPC2206 tested to failure under two different conditions. In all cases, each cycle consisted of a heating period of 30 seconds, followed by a cooling period of another 30 seconds. In Figure 49, information in red shows the devices that were cycled between 40°C and 100°C, and in green, the devices cycled between 40°C and 150°C. In both cases, solder fatigue is the only failure mechanism, so the slopes of the Weibull fits are almost the same. However, the Mean Time to Failure was strongly accelerated by the ΔT and T_{max} reached during each cycle.



Note: The parts with underfill (Namics U8437-2) are still under test with no failures after 53k cycles so the green Weibull "fit" represents a lower bound

Figure 49: Weibull plots of Intermittent Operating Life results of EPC2206

In addition, a third cohort of parts using underfill Namics U8437-2 was started cycling between 40°C and 150°C. After 53,000 cycles no failures were observed. The green line in Figure 49 assumes one failure after 53,001 cycles, and therefore can be viewed as a lower bound on the performance of this underfill. Clearly, as was found in the TC studies, the Namics underfill was found to affect a significant improvement (> 100x) in lifetime under cyclic temperature stress.

8.4 Finite Element Analysis

To better understand the key factors influencing thermo-mechanical reliability when using underfills, finite element simulations of EPC2206 under temperature cycling stress were conducted. Figure 50 shows the simulation deck used for this analysis. The die is placed on a 1.6 mm FR4 PCB, and the temperature change is ΔT = +100°C above the neutral (stress free) state. Two key underfill parameters were varied: Young's modulus and CTE. As shown in the figure, stress is analyzed along the cut line shown, providing visibility into the stress within the solder bars, die, and underfill.

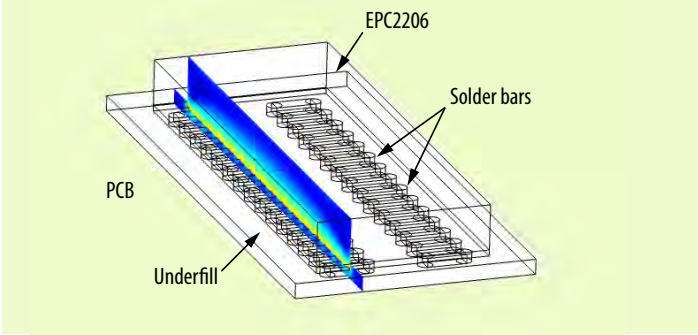


Figure 50: Simulation deck for finite element analysis of stresses inside EPC2206 under temp cycling stress. Die with underfill sitting on 1.6 mm FR4 PCB. Stress is analyzed along cut line shown.

Figure 51 shows the Von Mises [44], or peak shear stress, in the edgemost solder bar along the cutline. For clarity, only stress in the solder bar is shown. In addition, mechanical deformations are exaggerated by 20 times in order to illustrate the shear displacement in the joint. Four distinct underfill conditions are simulated by changing the Young's modulus (E) or the CTE of the underfill.

As can be seen, the solder bar in the no underfill case has by far the most extreme shear stress and deformation. The addition of underfill significantly alleviates stress from the joint, with the higher the E, the less stress in the joint. For underfills with poor CTE matching to the solder joint, stresses can also build up in the joint.

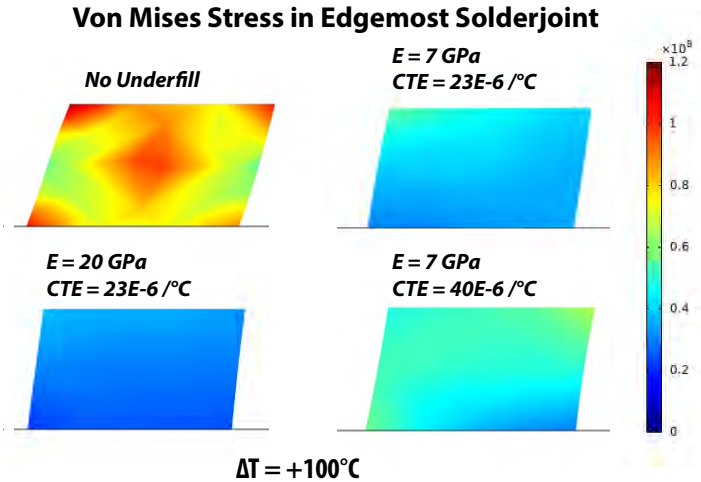


Figure 51: Von Mises (peak shear stress) in the edge-most solder bar under a temperature cycle change of ΔT = +100C. Four different underfill conditions are simulated, with changing Youngs modulus (E) of the underfill, and different CTE as well. Note that mechanical deformation has been exaggerated by 20x in all cases.

Figure 52 shows the same four conditions, but this time the Von Mises stress is shown in the die and underfill as well. As can be seen, the high Young's modulus cases show low stress in the solder joint, but high stress inside the die and underfill near the die edge. These high stresses can lead to cracking and ultimate failure inside the device.

FEA analysis shows that there is an optimal Young's modulus in the range of ~6 to 13 GPa, providing a good compromise between protecting the solder joint and protecting the die edge. With regard to CTE, the analysis shows that high underfill CTE (> 32) should be avoided.

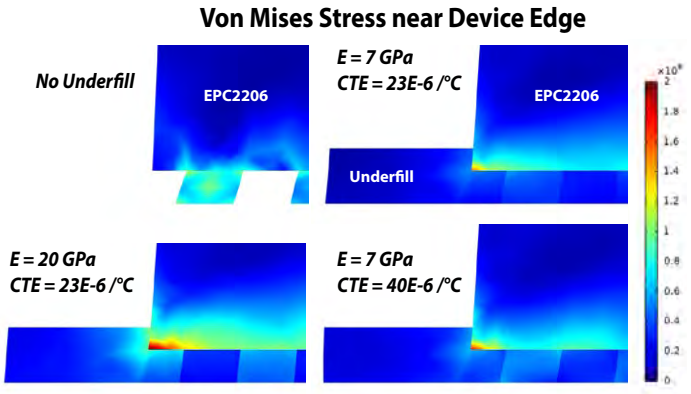


Figure 52: Von Mises (peak shear stress) in the edge-most solder bar under a temperature cycle change of ΔT = +100C. Four different underfill conditions are simulated, with changing Youngs modulus (E) of the underfill and different CTE as well. Note that deformation has been exaggerated by the same scale in each picture.

8.5 Guidelines for Choosing Underfill

The main guidelines for choosing an underfill for use with eGaN FETs are listed below:

Underfill CTE should be in the range of 16 to 32 ppm/°C, centered around the CTE of the solder joint (24 ppm/°C). Lower values within this range are preferred because they provide better matching to the die and PCB.

- Glass transition temperature (Tg) should be comfortably above the maximum operating temperature. When operated above Tg, the underfill loses its stiffness and ceases to protect the solder joint.
- Young's (or Storage) modulus in the range of 6–13 GPa. If the modulus is too low, the underfill is compliant and does not relieve stress from the solder joints. If it is too high, the high stresses begin to concentrate at the die edges.

From the experimental results in this study, Henkels UF1137_H and Namics 8410-406B and U8437-2_N underfills provide excellent boost in thermo-mechanical reliability when used with eGaN FETs.

SECTION 9: SUMMARY

GaN devices have been in volume production since 2010 and have demonstrated very high reliability in both laboratory testing and customer applications, such as lidar for autonomous cars, 4G base stations, vehicle headlamps, and satellites to name just a few. Test-to-fail testing can isolate intrinsic failure mechanisms and their behavior over all stress conditions. This information can then be used with confidence to predict device lifetime under a wide range of actual mission profiles.

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